YOUR DISCRETE TEST SOURCE
SCIENTIFIC TEST, INC.

2kV MODEL 5300C

CURVE TRACER and ATE SEMICONDUCTOR TESTER

CONTENTS

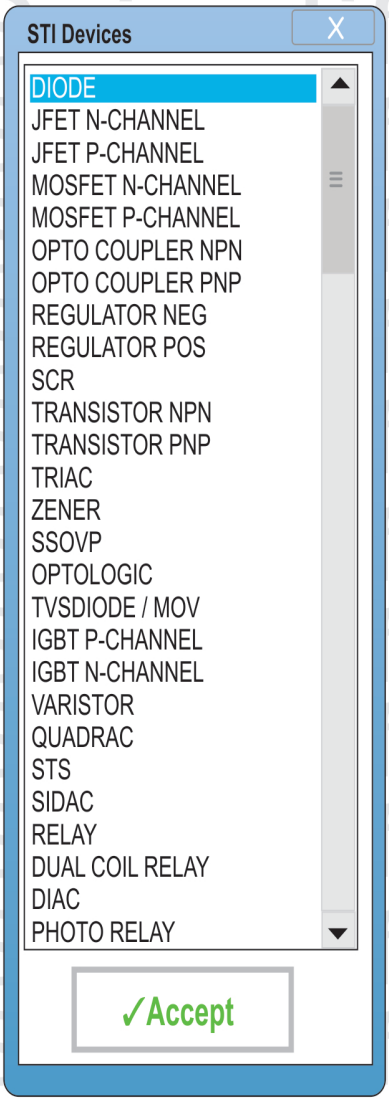
5300C ATE/CURVE TRACER

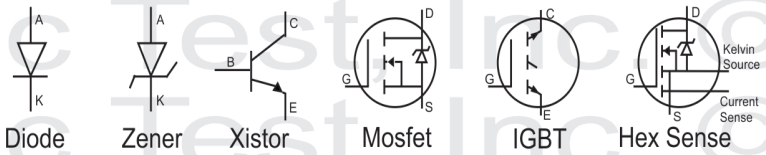
The Model 5300C ATE/CURVE TRACER provides all the functions of a full feature high speed ATE system plus CURVE TRACER capability.
Curves are generated using high speed ATE test steps to build the curve point by point. Precision data points are generated quickly and accurately. Data increments are programmable in linear or logarithmic steps. Curves are generated rapidly. Features include:

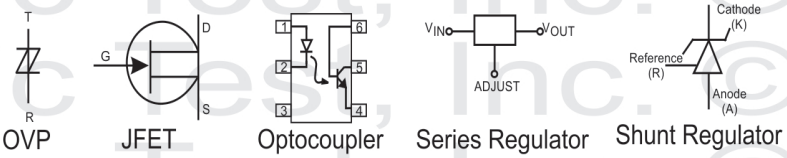
- Wide Selection of Available Curves
- High speed data capture ATE.
- RDSON to 1uΩ Resolution
- Optional Prober/Handler Interface
- Programmable Relay Drivers
- Auto Calibration
- Self-Test
- Programmable Data Point Increments on curves
- Increments can be Linear or Logarithmic
- Programmable Off-Time to Minimize Heating
- Load Curve Data Directly to Excel®
- Load ATE Data Directly to Excel®
- Run up to 10 Curve Programs in Sequence with data loaded to Excel® Automatically
- Logarithmic Curves
- No Patch Cords relay matrix makes all connections
- No SMU Set-Up-Selection; Completely Automatic
- GaN (HEMT) SiC Enhancement / Depletion Device

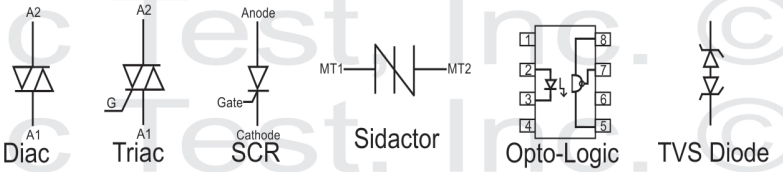
DEVICES TESTED

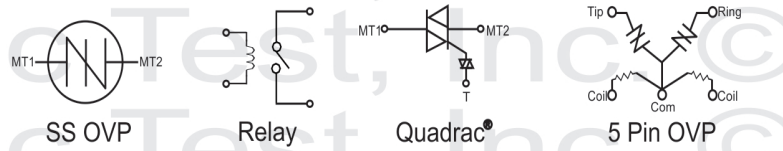
DEVICE FAMILIES



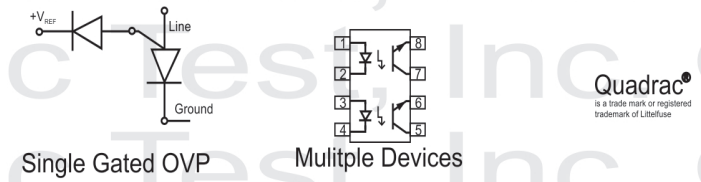








5 PIN MODULE I
5 PIN MODULE II
POS RAIL GATED OVP
NEG RAIL GATED OVP



Some Devices require Adaptors.

TESTS

MOSFET N/P CHANNEL

- VGSTH
- IDSS
- BVDSS
- VDSON
- IGSSF
- IGSSR
- VSD
- VGSF
- VGSR
- IDON
- VGSON
- RDSON
- CSRATIO
- CBVDSS

IGBT N/P CHANNEL

- VGETH
- ICES
- BVCES
- VCEON
- IGESF
- IGESR
- VGEON
- VF
- ICON
- CBVCES

DIODE

- VF
- IR
- BVR
- REV SRG
- CBVR

ZENER

- VF
- IR
- BVZ
- ZZ

OPTOCOUPLER NPN/PNP

- ICOFF
- ICBO
- BVCEO
- BVCBO
- HFE
- VCESAT
- IR
- VF
- CTR
- VSAT
- VF-
- CTR-
- VSAT-
- BVECO
- BVEBO
- hfe

JFET N/P CHANNEL

- VGSOFF
- IDSS
- BVDGO
- IGSS
- IDGO
- IDOFF
- BVGSS
- VDSON
- VGSON
- IDON
- RDSON

TESTS

TRANSISTOR NPN/PNP

- HFE
- VBE
- IEBO
- VCESAT
- ICBO
- ICE
- BVCE
- BVCBO
- BVEBO
- VBESAT
- VF
- RE
- VO
- hfe
- DVBE

REGULATOR POS/NEG

- Vout
- Iin
- VREF(POS Only)

SSOVP

- VCLAMP+
- VCLAMP-
- IBO+
- IBO-
- VBO+
- VBO-
- IH+
- IH-
- VT+
- VT-
- VZ+
- VZ-
- ID+
- ID-
- KELVIN

PHOTORELAY

- IOFF+
- IOFF-
- IR
- VF
- VON+
- VON-

OPTOLOGIC

- VF
- IR
- VOH
- VOL
- IFON
- IFOFF

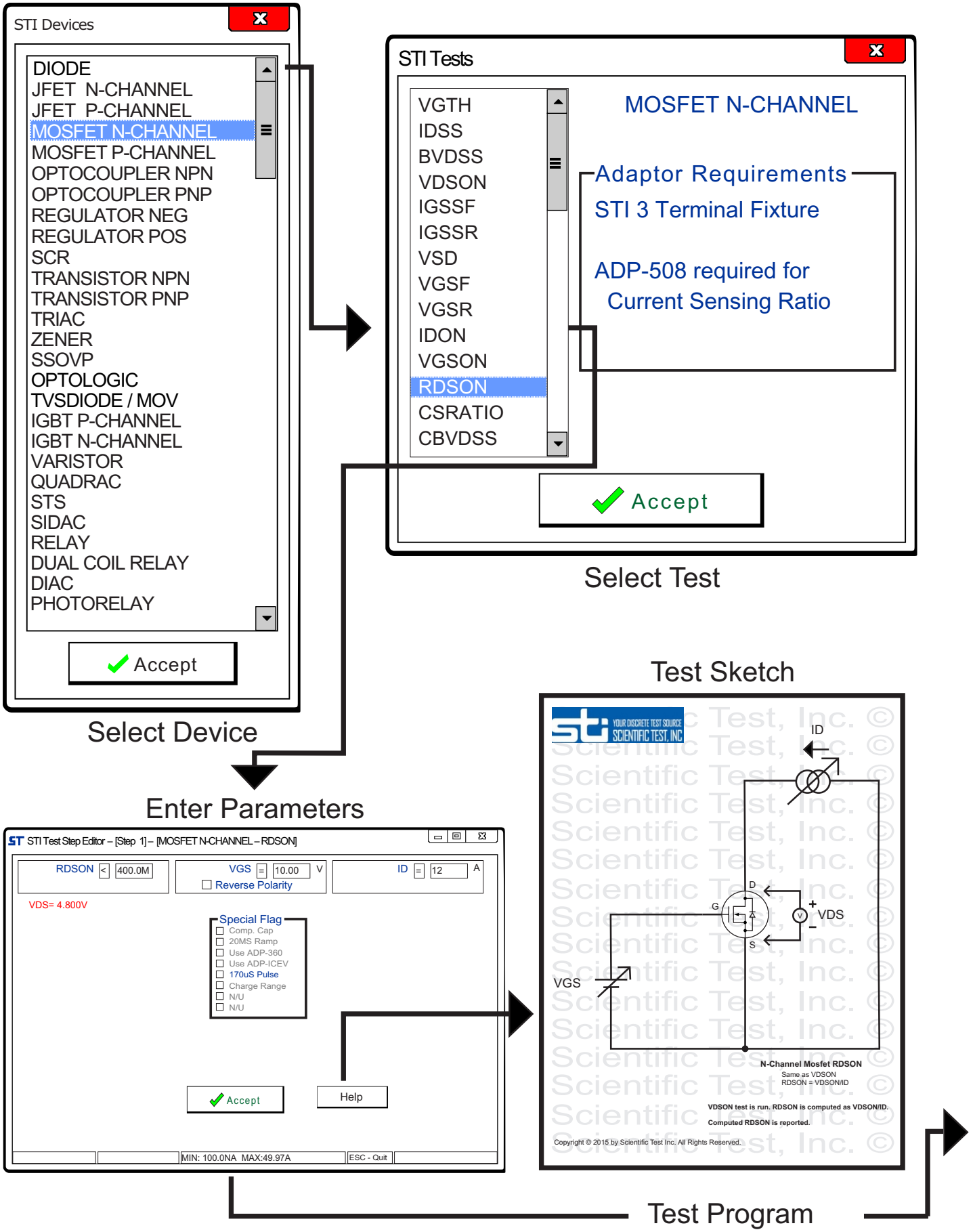
TRIAC

- IGT I
- IGT II
- IGT III
- IGT IV
- VGT I
- VGT II
- VGT III
- VGT IV
- IL+
- IL-
- IH+
- IH-
- VT+
- VT-
- VD+
- VD-
- IDRM
- IRRM
- VDRM
- VRRM

NOT SHOWN

SCR Quadrac® 5 Pin Modules TVS Diode/MOV
Varistor Sidac Gated OVP

TEST PROGRAMMING



TEST PROGRAMMING

Creating and editing test programs for the STI 5300C is both easy and intuitive. Each test program contains a series of test steps (these steps can be actual device tests or calculations), bin/sort plan, and if required, relay plan. Test steps are added or edited with a single or double mouse click. A device test window or calculation window is opened. In the device test window the limit parameter value is entered along with, if applicable, other bias voltages or currents (one of the biases can be a calculation), load resistors, etc. In the calculation window the calculation limit is entered along with the name and units to be used in displaying the results and then the actual calculation which may reference any test result from a previously entered device test. 96 test steps max.

BINNING / SORTING

By default all programmed test steps are set to pass on SORT/BIN 1. Each test step may be set for pass, fail or do not care for each sort. Each sort may be set to any of the logical bins. Binning and sorting can be as simple as running all of the programmed test steps and then finding the first qualifying sort or as complex as branching on the first non-qualifying test to the next valid sort. In this more complex mode it is quite possible that only a subset of the programmed tests will be run on a given device and that all devices tested may not run the same subset of test steps 99 sorts max.

EXTERNAL RELAYS FOUR PLUS OPTIONAL FIFTEEN

Four to fifteen (depending upon options supplied with the STI tester) relay drivers can be assigned to any programmed test step. These relay drivers can be used to provide external loads or connections for a given device test.

TEST PROGRAM

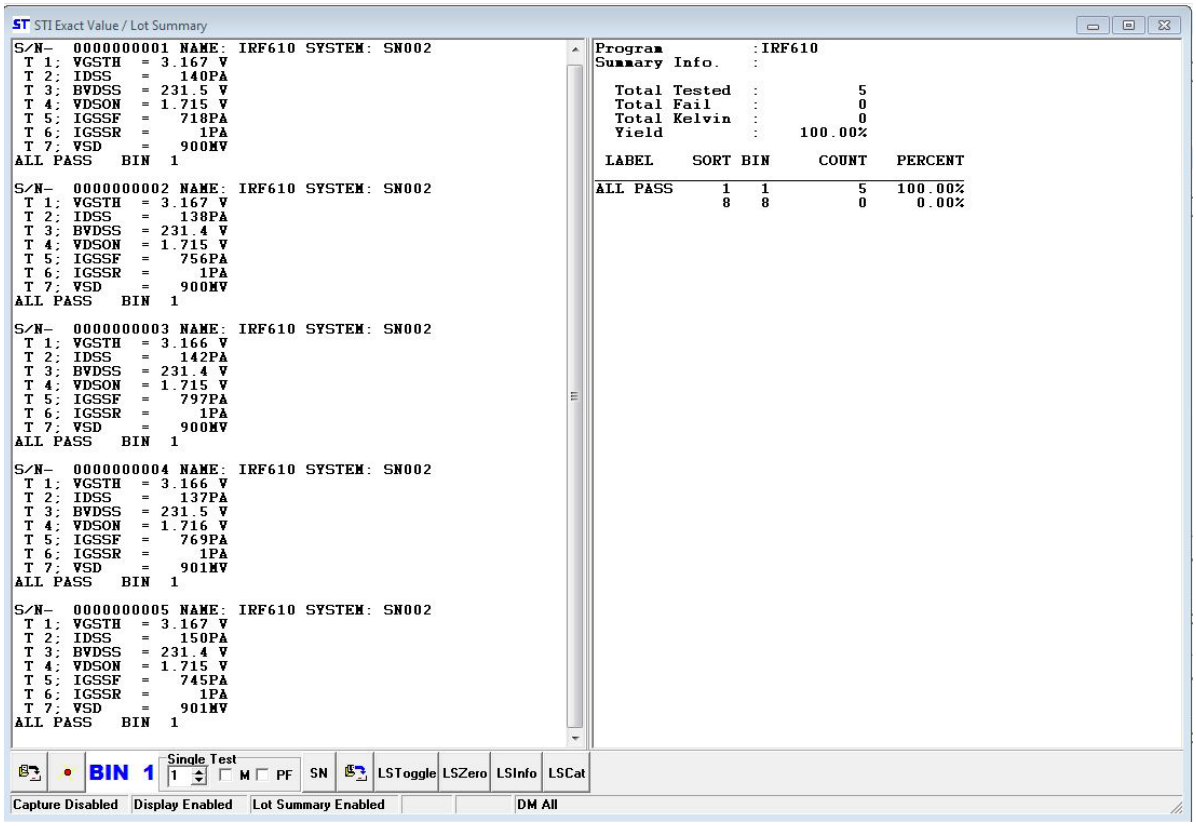
ST Test Program – E:\RDSON.T60

Test Steps (4) | Options | Bin / Sort Plan | Relay Plan | Ext. Relay Plan | ADP-401 Scanner Plan

Step:Scan			Device	Limit	Bias 2	Bias 3	RBE/RGK	RL	RGS	BP	ANET	GNET	Soak	R...
01:00	DL	AR	MOSFET N-CHANNEL	VGSTH < 5.000 V	ID = 250.0UA									
02:00	DL	AR/D	MOSFET N-CHANNEL	IDSS < 20.00UA	VDS = 800.0 V								0	Off
03:00	DL	AR/D	MOSFET N-CHANNEL	IGSSF < 100.0NA	VGSF = 20.00 V	A			Short				0	
04:00	DL	AR	MOSFET N-CHANNEL	RDSON < 400.4M	VGS = 10.00 V	ID = 12.00 A								
05:00	DL	AR	MOSFET N CHANNEL	BVDSS > 900.0 V	ID = 250.0UA						Off		Off	
i 06:00		AR	MOSFET N-CHANNEL	VGSON < 9.000 V	VDS = 8.000 V	ID = 7.987 A								
i 07:00		AR	MOSFET N-CHANNEL	VGSON < 9.000 V	VDS = 8.000 V	ID = 6.013 A								
08:00	DL		Calculation	GFS > 4.000	GFS = (7.987e+00 - 6.013e+00) / (s6 - s7)									

2KV ATE

LOGGED DATA



DATA TO EXCEL ®

Operator										
Station										
Product										
Process										
Start Date	22/08/2023	02:29:21 p.m.								
Finish Date										
Part Number										
Remarks										
E:\5300C_LODECK\IRF610.DAT										
Serial Number	Label	Sort	Bin	1) VGSTH [V]	2) IDSS [A]	3) BVDSS [V]	4) VDSON [V]	5) IGSSF [A]	6) IGSSR [A]	7) VSD [V]
				VGSTH > 2.002 V	IDSS < 250.2UA	BVDSS > 200.7 V	VDSON < 3.843 V	IGSSF < 500.2NA	IGSSR < 500.2NA	VSD < 2.002 V
				ID = 250.2UA	VDS = 200.7 V	ID = 250.2UA	VGS = 10.03 V	VGSF = 20.02 V	VGSR = 20.02 V	IS = 3.301 A
							ID = 1.601 A			
1	ALL PASS		1	3.074	159.0E-12	230.9	1.708	860.0E-12	1.000E-12	888.0E-03
2	ALL PASS		1	3.075	150.0E-12	230.8	1.709	930.0E-12	1.000E-12	888.0E-03
3	ALL PASS		1	3.076	139.0E-12	230.8	1.708	952.0E-12	1.000E-12	888.0E-03
4	ALL PASS		1	3.076	142.0E-12	230.8	1.708	947.0E-12	1.000E-12	888.0E-03
5	ALL PASS		1	3.076	140.0E-12	230.8	1.709	959.0E-12	1.000E-12	888.0E-03
	N			5	5	5	5	5	5	5
	Minimun			3.074	139.0E-12	230.8	1.708	860.0E-12	1.000E-12	888.0E-03
	Range			2.000E-03	20.00E-12	100.00E-03	1.000E-03	99.00E-12	000.000E+00	000.000E+00
	Maximum			3.076	159.0E-12	230.9	1.709	959.0E-12	1.000E-12	888.0E-03
	Mean			3.075	146.0E-12	230.8	1.708	929.6E-12	1.000E-12	888.0E-03
	Std. Deviation			894.4E-06	8.456E-12	44.72E-03	547.7E-06	40.35E-12	000.000E+00	124.13E-18
	Variance			800.0E-09	71.50E-24	2.000E-03	300.0E-09	1.628E-21	000.000E+00	15.4E-33

CURVES - EXAMPLES

Mosfet N/P Channel
- ID vs. VDS (at range of VGS)
- ID vs. VGS (at range of VDS)
- IS vs. VSD
- RDS vs. VGS (at fixed ID)
- RDS vs. ID (at several VGS)
- IDSS vs. VDS (Reverse Bias Selectable)
- VGSTH vs. ID
- IGSS vs. VGS

Transistor NPN / PNP
- HFE vs. IC
- BVCE(O,S,R,V) vs. IC
- BVEBO vs. IE
- ICBO vs. VCBO
- VCE(SAT) vs. IC (at fixed IC/IB ratio)
- VCE(SAT) vs. IB (at range of IC)
- VBE(SAT) vs. IC (at fixed IC/IB ratio)
- VBE(ON) vs. IC (at fixed VCE)
- IC vs. VCE (at range of IB)(Curve Tracer only)
- IEBO vs. VEB
- ICEO vs. VCE

IGBT N/P Channel
- IC vs. VCE (at range of VGE)
- IC vs. VGE (at range of VCE)
- ICES vs. VCE
- IF vs. VF
- VCE vs. VGE

Diode
- IF vs. VF
- IR vs. VR

Zener
- IF vs. VF
- IZ vs. BVZ

TRIAC
- IT vs. VT+ (at fixed IG and RGK open)
- IT vs. VT- (at fixed IG and RGK open)

SCR
- IT vs. VTM (at fixed IG and RGK open)

SSOVP
- IT vs. VT+ (at fixed IBO)
- IT vs VT- (at fixed IBO)

SIDAC
- IT vs. VT+ (at fixed IBO)
- IT vs VT- (at fixed IBO)

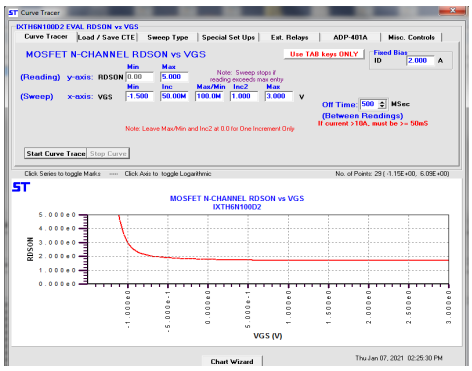
DIAC
- ID vs. VF+
- ID vs. VF-

Regulator Positive
- Electronic Load vs. VOUT (at fixed IMAX)

Regulator Negative
- Electronic Load vs. VOUT (at fixed IMAX)

JFET N/P Channel
- ID(OFF) vs. VDS (at range of VGS)
- ID(OFF) vs. VGS (Reverse Bias) (at fixed VDS)
- ID(ON) vs. VDS (at range of VGS)
- ID(ON) vs. VGS (Reverse Bias) (at fixed VDS)

Other Curves
- V vs. I Quadrants I and III
- I vs. V Quadrants I and III

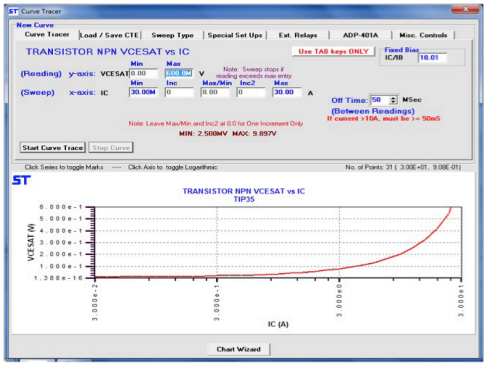


NMOS RDSON vs VGS (Figure 1)
Depletion Mode Device

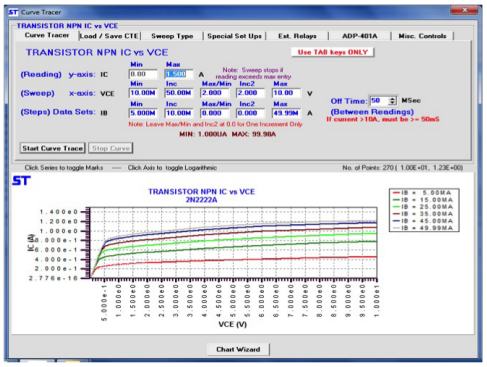
NPN hFE vs IC (Figure 2)

N JFET, IDON vs VDS (Figure 3)

CURVE SUITE (Figure 4)



NPN VCESAT vs IC, IC/IB Fixed Ratio
(Figure 5)



NPN IC vs VCE (Figure 6)

CURVE DATA TO EXCEL®

Notes:
MOSFET N-CHANNEL IDON vs VDS

VGS = 2.400V		VGS = 2.450V		VGS = 2.500V		VGS = 2.550V		VGS = 2.599V	
IDON	VDS	IDON	VDS	IDON	VDS	IDON	VDS	IDON	VDS
0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
239.0E-03	10.000E-03	299.1E-03	10.000E-03	353.9E-03	10.000E-03	392.6E-03	10.000E-03	454.8E-03	10.000E-03
1.191	60.00E-03	1.857	60.00E-03	2.713	60.00E-03	3.836	60.00E-03	5.163	60.00E-03
1.469	110.0E-03	2.331	110.0E-03	3.570	110.0E-03	5.224	110.0E-03	7.308	110.0E-03
1.580	160.0E-03	2.548	160.0E-03	3.942	160.0E-03	5.825	160.0E-03	8.349	160.0E-03
1.640	210.0E-03	2.645	210.0E-03	4.119	210.0E-03	6.185	210.0E-03	8.898	210.0E-03
1.682	260.0E-03	2.725	260.0E-03	4.260	260.0E-03	6.393	260.0E-03	9.234	260.0E-03
1.713	310.0E-03	2.777	310.0E-03	4.342	310.0E-03	6.533	310.0E-03	9.466	310.0E-03
1.734	360.0E-03	2.825	360.0E-03	4.412	360.0E-03	6.649	360.0E-03	9.643	360.0E-03
1.754	410.0E-03	2.856	410.0E-03	4.476	410.0E-03	6.738	410.0E-03	9.771	410.0E-03
1.774	460.0E-03	2.883	460.0E-03	4.516	460.0E-03	6.814	460.0E-03	9.893	460.0E-03
1.777	500.0E-03	2.902	500.0E-03	4.547	500.0E-03	6.848	500.0E-03	9.963	500.0E-03
1.956	2.500	3.189	2.500	5.007	2.500	7.556	2.500	10.90	2.500
2.053	4.500	3.332	4.500	5.242	4.500	7.888	4.500		
2.133	6.500	3.463	6.500	5.447	6.500	8.242	6.500		
2.212	8.500	3.604	8.500	5.679	8.500	8.566	8.500		
2.270	10.00	3.695	10.00	5.807	10.00	8.764	10.00		

CURVE PROGRAMMING

Curve tracer programming is illustrated in Figure 7 below which shows entries for and IDON vs VDS N Chan MOSFET. IDON and VDS start and end points plus increment sizes are entered. VGS increments determine the number of IDON vs VDS sweeps.

Additional tabs provide user selectable features including sweep type, programmable relay drivers, and load to an Excel® file including graph and data points.

A number of graphing features are also included. The mouse can be used to zoom in on a specific area of the curve. Cursors can be moved on a completed curve to re-set start and stop limits to re-generate the curve in greater detail in an area of interest. Clicking on an axis will change the scale from linear to logarithmic. Clicking on a curve will show all data points on the curve.

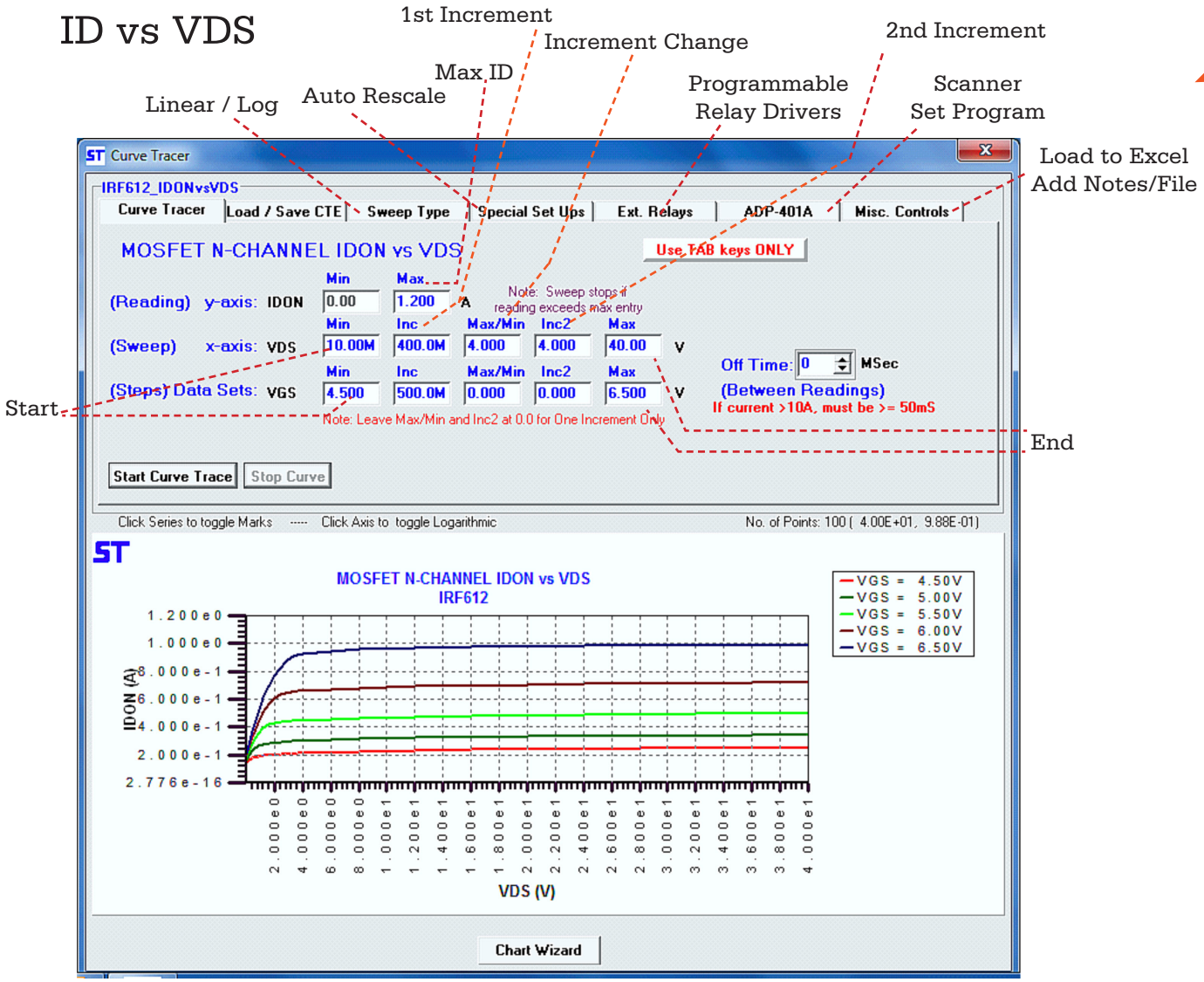


Figure 7

Other curves are similarly programmed.

TEST SPECIFICATIONS

SCIENTIFIC TEST, INC. TEST SPECIFICATIONS 5300C

TEST		SPECIFICATION			
	PARAMETER	V RANGE	I RANGE	MAX RES.	ACCURACY
LEAKAGE	I_R, I_{CBO}, $I_{CEO/R/S/X}$, $I_{DSS/X}$, I_{DOFF}, I_{DRM}, I_{RRM}	2000V	2NA (20PA)[3] to 50MA	0.1 NA (1PA)[3]	1% + 2NA + 20PA/V (1% + 200PA + 2PA/V)[3,4]
	I_{EBO}, I_{GSSF}, I_{GSSR}, I_{GSS}, I_{GKO}, I_R (OPTO)	.10V to 20V (80V)[2]	2NA to 3A	0.1 NA	1% + 2NA + 20PA/V (1% + 200PA + 2PA/V)[3,4]
BREAKDOWN	TRANSISTOR BV_{CEO}, BV_{CES} (300µS Pulse above 10mA)	.10V to 500V to 1400V to 1600V	100µA to 999.9MA to 100MA to 50MA	1 MV	1% + 100MV
	BV_{DSS}, V_D, BV_{CBO}, BV_{CES} (IGBT), V_{DRM}, V_{RRM}, V_{BB}, BV_R	.10V to 2000V	100NA to 50MA	1 MV	1% + 100MV
	BVZ	.10V to 5.00V to 9.999V to 50.00V to 1000V BVZ Soak - 50V 0-50 ms 0- 99 sec	10µA to 49.9A to 25A to 9.99A to 100 MA to 400MA to 80 MA	1 MV	0.4% + 2 LSB
	BV_{EBO}, BV_{GSS}, BV_{GKO}	.10V to 20V (80V)[5]	100NA to 3A	1 MV	1% + 10MV
VCESUS	V_{CEOSUS}, V_{CERSUS}, V_{CEVSUS}	V_{CE}: TO 1500V Inductive Kickback, 35mH choke	I_C: to 4A	0.5V	2% + 0.5V
IMPEDANCE	ZZ (1 kHZ) 0.1Ω to 20 KΩ	0.1V to 200V DC (measure 50µV to 300mV rms)	100µA to 300mA	0.001 Ω 1µV	1% + 1% Range
GAIN	h_{FE} (1 to 99,999) CTR (.01 to 99,999) gFS, gFE	V_{CE}: .10V to 5.00V to 9.99V to 49.9V VDS, ID: Same as ON STATE VGS: 0.1V to 20V (80V)[2]	I_E: 10µA to 49.9A (99.9A) derate to 25A (50A) derate to 9.99A I_F, I_B: 100NA to (10A) ΔID/ΔVGS automatically computed	.01 hFE .0001 CTR	V_{CE}: 1% + 10MV I_C: 1% + 100NA I_F, I_B: 1% +5NA

Optional High Current:

-100A Option (1)
-High Current Deck: 1200
-80V Low Source Option (2)
-Low Current Deck (3)
-(1% + 2NA + 40PA)(4) High Deck or Adapter

TEST SPECIFICATION

	PARAMETER	V RANGE	I RANGE	MAX RES.	ACCURACY
ON STATE	V_{CESAT}, V_{BESAT}, V_{BEON} V_F, V_T V_{DSON}, I_{DON}, V_{GSON} V_{GEON} V_F (Opto-Diode)	V_{CE}, V_D, V_F, V_T: .10V to 5.00V to 9.99V V_{GS}, V_{GE}, V_{BE}, V_F: .10V to 9.99V	I_E, V_T, I_F, I_D: 10µA to 49.9A (99.9A)[1] derate to 25A (50A)[1] I_B, I_F, I_{GT}: 100NA to 10A	1MV	V: 1% + 10MV I_E, I_F, I_D, I_T: 1% + 100NA I_B, I_{GT}: 1% + 5NA
	RDSON	500µΩ to 1KΩ	VDS, ID: Same as ON STATE VGS: 0.1V to 80V[2]	1µΩ	4% + (0.5MV/ID)Ω
	V_{GSTH}, V_{GETH}	.10V to 49.9V	I_D: 100µA to 3A	1MV	1% + 10MV
	V_O (Regulator)	V_O: .10V to 80V V_{IN}: .10V to 49.9V Load: Resistive or Electronic	I_O: 1MA to 5A	1MV	1% + 10MV
	I_{IN} (Regulator)	V_{IN}: .10V to 80V[2] Load: R_{GK}, 1K, 10K, EXT, OPEN, SHORT	I_{IN}: 1MA to 3A	10NA	1% + 5NA
	V_C	.10V to 49.9V	10MA to 10A	1MV	1% + 10MV
OFF	V_{GSOFF}	V_O: .10V to 80V	I_D: 100NA (20PA) to 3A V_{DS}: .10V to 50V	1MV	1% + 10MV
TRIGGER	I_{GT} V_{GT} V_{OPER} (Relay)	V_D: 5V to 49.9V V_{GT}: .10V to 80V .10V to 50V	I_{AK}: to 3A I_{GT}: 100NA to 3A R_L: 12, 30, 100Ω, EXT	10NA 1MV .10V	1% + 5NA 1% + 10MV 1% + .10V
HOLD	I_H $V_{RELEASE}$ (Relay)	V_D: 5V to 49.9V .10V to 50V	I_H: 1.5A I_{GT}: 100NA to 3A R_L: 12, 30, 100Ω, EXT (Initial I_{AK} set by R_L)	1µA .10V	1% + 2µA 1% + .10V
LATCH	I_L (ADP-506 required for exact value)	V_D: 5V to 49.9V	I_L: 100µA to 3A I_{GT}: 100NA to 3A R_L: 12, 30, 100Ω, EXT	N/A	N/A
BREAKOVER	V_{BO}, I_{BO} (SSOVP) V_{BO}, I_{BO} (STS, DIAC) V_{BO}, I_{BO} (SIDAC) V_S, I_S (SBS, STS)	0.10 to 400V 0.10 to 80V 0.10 to 400V 0.10 to 80V	10mA to 900mA 1µA to 200µA 1µA to 1mA 1µA to 200µA	1mV	1% + 100mV 1% + 10mV 1% + 100mV

Accuracy specifications are in addition to ± 2 digit in readout. +/- 0.02% Range.

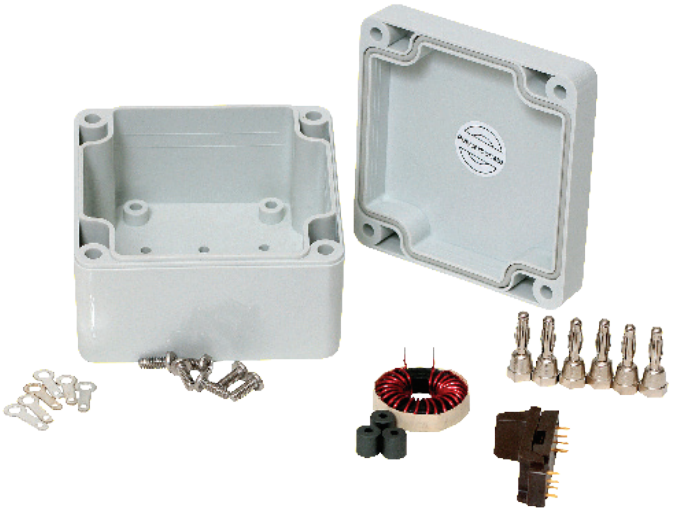
Adaptors

- 16 Pin Programmable Scanner
- Regulator
- Opto Logic
- Gated Device
- Opto Coupler
- Sidac/Diac/SSOVP
- 4 Quadrant ILatch, IH, VT
- Low Current Deck (1 PA Resolution)

FIXTURES

A selection of fixtures is available, including:

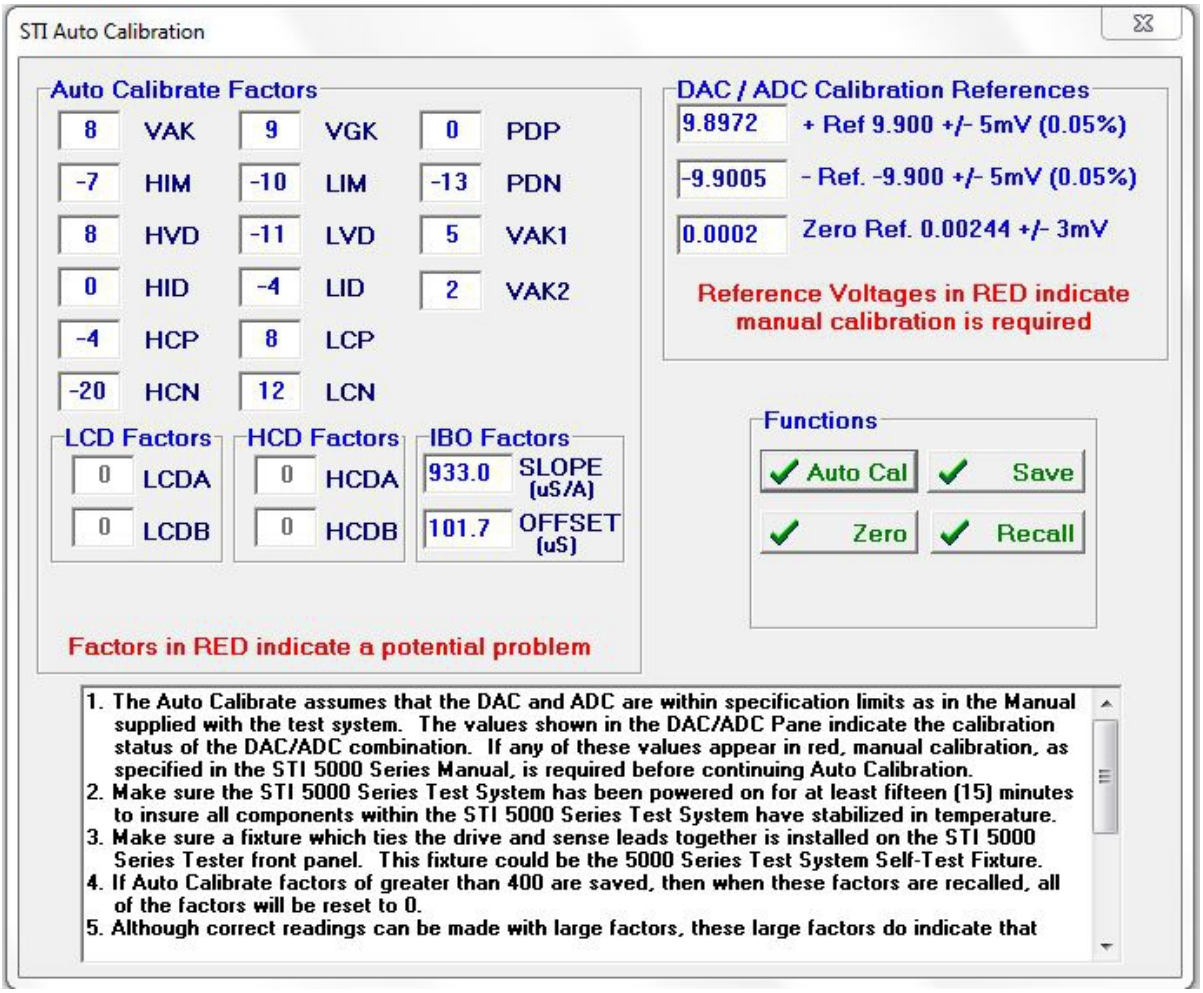
- TO-220/218
- TO-72
- TO-5/18
- TO-92
- TO-3/66
- Axial (small and large)
- DP-4/5
- 8 Pin DIP
- 6 Pin TO-5
- SOT-23, SOT-24, SOT-25, SOT-26
- D-PAK
- TO-252
- SOT-89
- TO-243
- D2-PAK
- SOT-223
- TO-261
- SMA
- SMB
- SMC
- MELF (MINI-MELF, MICRO-MELF)
- SO-4, SO-6, SO-8, SO-16
- SOD-123, SOD-323, SOD-80
- Custom Fixtures
  (made for any device type for which a socket is commercially available)
- Blank



DIAGNOSTICS / AUTO CALIBRATION

The STI Tester provides extensive diagnostics for the Mainframe, Low Current Deck, Pin Programmable Scanner and OVP/Gated OVP adaptor. These self test diagnostics are built into the tester code, and with the supplied self test fixture, can be run at any time.

In addition, the STI Tester has an extensive auto calibration procedure that provides the user the ability to track calibration trends, verify that the DAC/ADC combination is functioning correctly, and supply calibration factors that will automatically correct the test result.



FEATURES

Auto-Calibrate
Self-Test
GaN (HEMT)
SiC
Enhancement/Depletion Tests and Curves
Relay Drivers
Datalog to Excel©
Curve Data to Excel©
1 Microhm RDSON Resolution
Fixture Selection
Prober/Handler Interface Option
80V Gate
1KHZ Zener Impedance

CONTACT

For More Information Please Contact:

Scientific Test, Inc.,
809 Boaz Circle Suite 160
Wylie, TX 75098-4705
www.scitest.com
PH: 469-969-0212
Email: Sales@scitest.com or info@scitest.com

Scientific Test, Inc., 809 Boaz Circle Suite 160, Wylie, TX 75098
VOICE: 469-969-0212 | FAX: 469-969-0221| info@scitest.com | www.scitest.com

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