

**Acute**<sup>®</sup>  
PC-based T&M Instruments

# Electrical Validation Documents

USER



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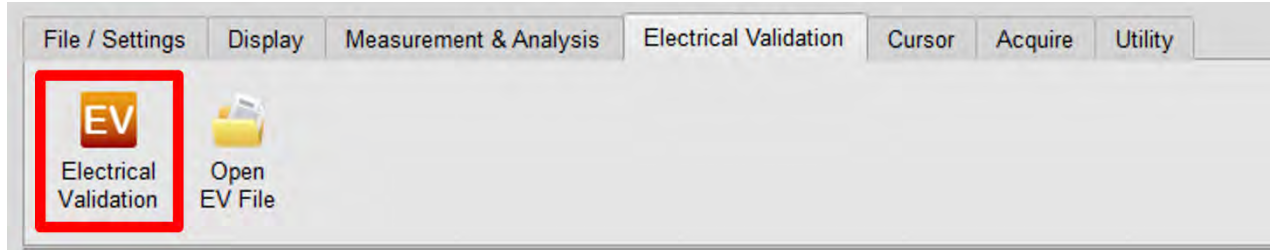
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# I2C Electrical Validation Solution

## ■ Introduction:



Use an oscilloscope to do I2C Electrical Validation to ensure that the I2C meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

I2C Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the I2C Speed.

Part of the electrical characteristics of common I2C specifications:

Table 13. Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I<sup>2</sup>C-bus devices<sup>[1]</sup>

| Symbol              | Parameter  | Conditions | C <sub>b</sub> = 100 pF (max) |     | C <sub>b</sub> = 400 pF <sup>[2]</sup> |     | Unit |
|---------------------|--|------------|-------------------------------|-----|--|-----|------|
|                     |  |            | Min                           | Max | Min                                    | Max |      |
| f <sub>SCLH</sub>   | SCLH clock frequency   |            | 0                             | 3.4 | 0                                      | 1.7 | MHz  |
| t <sub>SU,STA</sub> | set-up time for a repeated START condition   |            | 160                           | -   | 160                                    | -   | ns   |
| t <sub>HD,STA</sub> | hold time (repeated) START condition   |            | 160                           | -   | 160                                    | -   | ns   |
| t <sub>LOW</sub>    | LOW period of the SCL clock  |            | 160                           | -   | 320                                    | -   | ns   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock   |            | 60                            | -   | 120                                    | -   | ns   |
| t <sub>SU,DAT</sub> | data set-up time   |            | 10                            | -   | 10                                     | -   | ns   |
| t <sub>HD,DAT</sub> | data hold time   |            | 0 <sup>[3]</sup>              | 70  | 0 <sup>[3]</sup>                       | 150 | ns   |
| t <sub>rCL</sub>    | rise time of SCLH signal   |            | 10                            | 40  | 20                                     | 80  | ns   |
| t <sub>rCL1</sub>   | rise time of SCLH signal after a repeated START condition and after an acknowledge bit |            | 10                            | 80  | 20                                     | 160 | ns   |
| t <sub>fCL</sub>    | fall time of SCLH signal   |            | 10                            | 40  | 20                                     | 80  | ns   |

The report of common I2C validation:

| Name       | Description                                      | Limit Min  | Limit Max   | Min         | Mean        | Max         | Count | Result |
|------------|--|------------|-------------|-------------|-------------|-------------|-------|--------|
| f_SCL      | SCL clock frequency                              | 0.000 KHz  | 400.000 KHz | 387.596 KHz | 387.683 KHz | 387.897 KHz | 34200 | Pass   |
| t_HOLDSTA  | Hold time(repeated) START condition              | 600.000 ns | ---         | 1.536 us    | 1.537 us    | 1.540 us    | 200   | Pass   |
| t_HOLDSTA  | Set-up time for a repeated START condition       | 600.000 ns | ---         | 2.010 us    | 2.012 us    | 2.014 us    | 100   | Pass   |
| t_HOLDAT   | Data hold time                                   | ---        | ---         | 94.000 ns   | 274.110 ns  | 1.028 us    | 17250 | Pass   |
| t_HOLDAT   | Data Set-up time                                 | 100.000 ns | ---         | 472.000 ns  | 1.066 us    | 1.444 us    | 25100 | Pass   |
| t_HOLDSTO  | Set-up time for STOP condition                   | ---        | ---         | ---         | ---         | ---         | 0     | ---    |
| f_CLOCK    | Low Period of the SCL Clock                      | 1.300 us   | ---         | 1.538 us    | 1.542 us    | 1.544 us    | 34100 | Pass   |
| f_CLOCK    | High Period of the SCL Clock                     | 600.000 ns | ---         | 974.000 ns  | 982.475 ns  | 3.560 us    | 41800 | Pass   |
| t_RISE_SCL | Rise time of SCL signal                          | 20.000 ns  | 300.000 ns  | 45.999 ns   | 50.304 ns   | 51.999 ns   | 41800 | Pass   |
| t_FALL_SCL | Fall time of SCL signal                          | 20.000 ns  | 300.000 ns  | 10.000 ns   | 10.528 ns   | 11.999 ns   | 41800 | Fail   |
| t_RISE_SDA | Rise time of SDA signal                          | 20.000 ns  | 300.000 ns  | 37.999 ns   | 39.210 ns   | 41.999 ns   | 9300  | Pass   |
| t_FALL_SDA | Fall time of SDA signal                          | 20.000 ns  | 300.000 ns  | 4.000 ns    | 6.714 ns    | 10.000 ns   | 9900  | Fail   |
| t_BTF      | Bus free time between a STOP and START condition | ---        | ---         | ---         | ---         | ---         | 0     | ---    |
| t_VALIDAT  | Data valid time                                  | ---        | 900.000 ns  | 98.000 ns   | 267.062 ns  | 1.068 us    | 15750 | Fail   |
| t_VALIDACK | Data valid acknowledge time                      | ---        | 900.000 ns  | 98.000 ns   | 623.009 ns  | 1.068 us    | 1500  | Fail   |

Dedicated page for Electrical Validation:



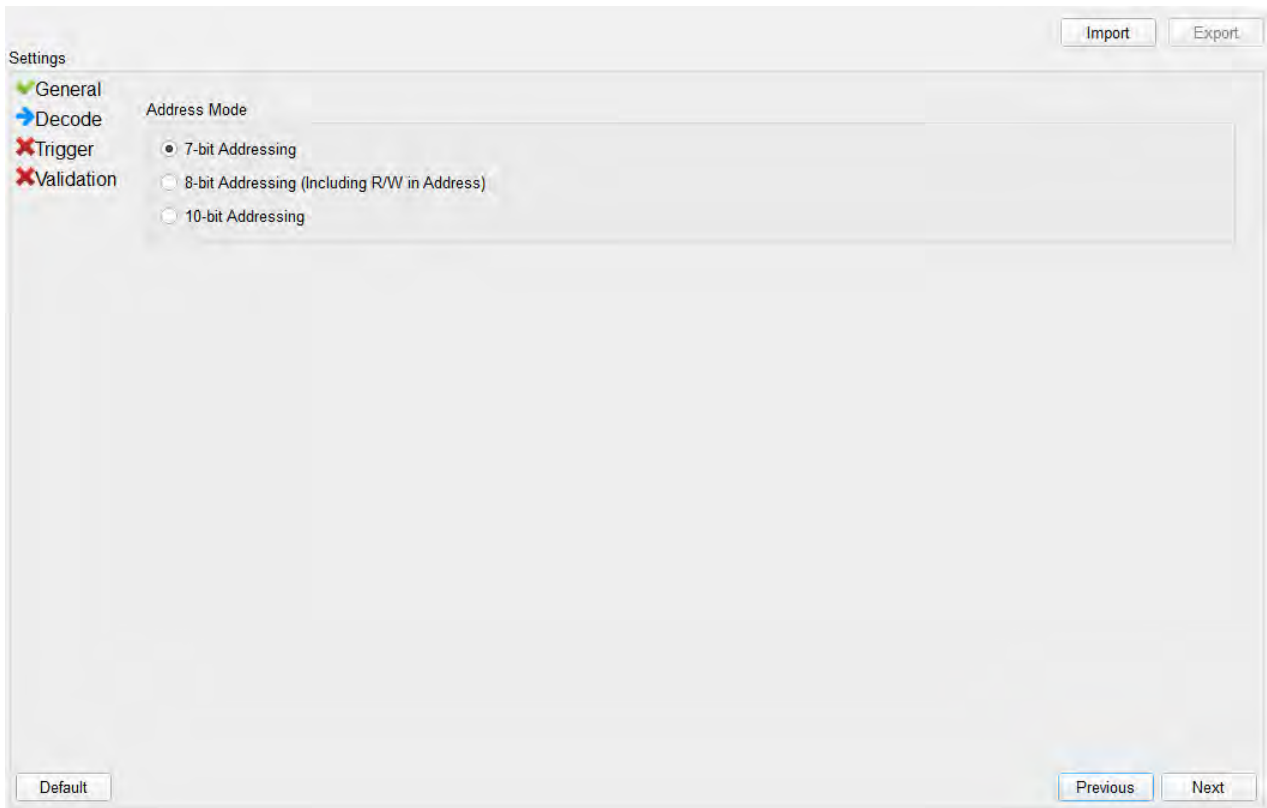
1. Different Speed Mode including Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
2. Frequency: Clock speed
3. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
4. Voltage: V\_IL, V\_IH, etc.

## I2C Electrical Validation Settings:

### 1. General Settings: Channel sources, working voltage and speed



### 2. Decode Settings: I2C decoding settings



### 3. Trigger Settings: I2C Address, Data trigger condition

Settings

- ✔ General
- ✔ Decode
- ➔ Trigger
- ✘ Validation

Trigger Settings

7-bit Address:

Write/Read:

ACK/NACK:

Data

Any Offset  Fixed Offset

Value

|                                  |                                  |
|----------------------------------|----------------------------------|
| <input type="text" value="XXh"/> | <input type="text" value="---"/> |
| <input type="text" value="XXh"/> | <input type="text" value="---"/> |
| <input type="text" value="XXh"/> | <input type="text" value="---"/> |
| <input type="text" value="XXh"/> | <input type="text" value="---"/> |

Default Previous Next

### 4. Electrical validation settings: Voltage, timing, frequency limitation

Import Export

Settings

- ✔ General
- ✔ Decode
- ✔ Trigger
- ➔ Validation

Customized EV Parameter:

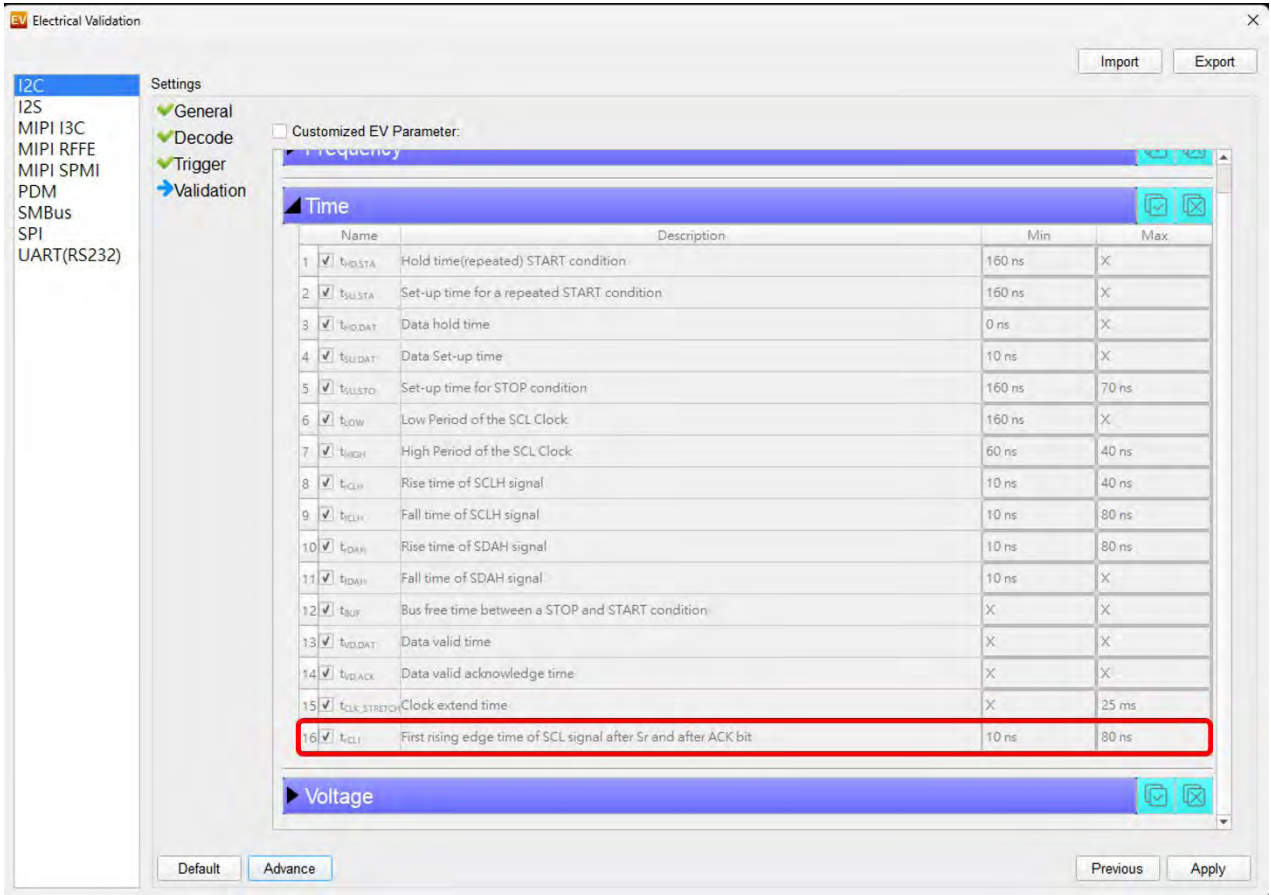
**Frequency**

| Name   | Description         | Min   | Max     |
|--|---------------------|-------|---------|
| 1 <input checked="" type="checkbox"/> f <sub>SCL</sub> | SCL clock frequency | 0 kHz | 100 kHz |

**Time**

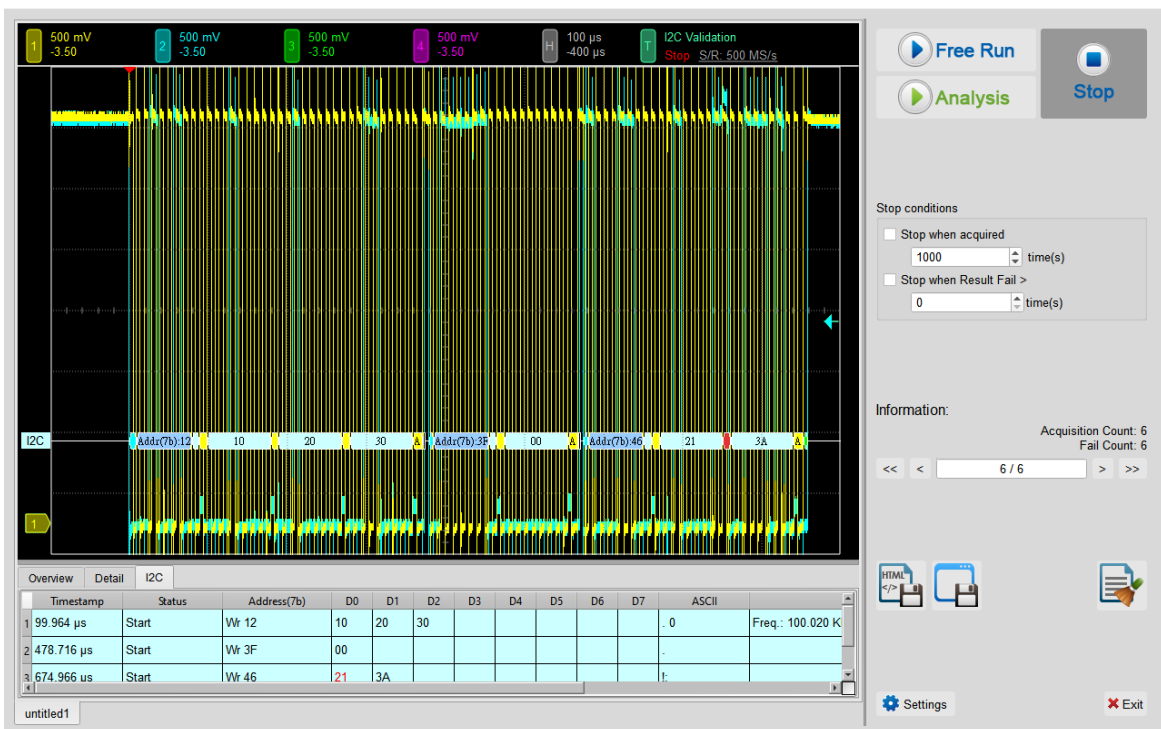
| Name   | Description                                | Min    | Max    |
|--|--|--------|--------|
| 1 <input checked="" type="checkbox"/> t <sub>HO,STA</sub>  | Hold time(repeated) START condition        | 4 us   | X      |
| 2 <input checked="" type="checkbox"/> t <sub>SU,STA</sub>  | Set-up time for a repeated START condition | 4.7 us | X      |
| 3 <input checked="" type="checkbox"/> t <sub>HO,DATA</sub> | Data hold time                             | 5 us   | X      |
| 4 <input checked="" type="checkbox"/> t <sub>SU,DATA</sub> | Data Set-up time                           | 250 ns | X      |
| 5 <input checked="" type="checkbox"/> t <sub>SU,STOP</sub> | Set-up time for STOP condition             | 4 us   | X      |
| 6 <input checked="" type="checkbox"/> t <sub>LOW</sub>     | Low Period of the SCL Clock                | 4.7 us | X      |
| 7 <input checked="" type="checkbox"/> t <sub>HIGH</sub>    | High Period of the SCL Clock               | 4 us   | X      |
| 8 <input checked="" type="checkbox"/> t <sub>CL</sub>      | Rise time of SCL signal                    | X      | 1 us   |
| 9 <input checked="" type="checkbox"/> t <sub>FL</sub>      | Fall time of SCL signal                    | X      | 300 ns |
| 10 <input checked="" type="checkbox"/> t <sub>DA</sub>     | Rise time of SDA signal                    | X      | 1 us   |
| 11 <input checked="" type="checkbox"/> t <sub>FDA</sub>    | Fall time of SDA signal                    | X      | 300 ns |

Default Advance Previous Apply

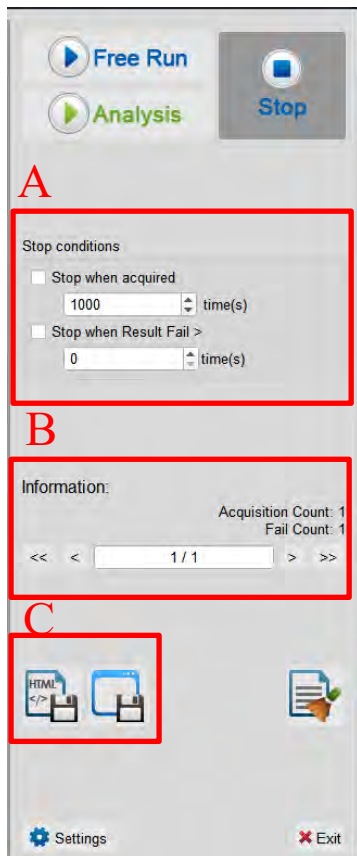


The 16<sup>th</sup> option can only be seen while the I<sup>2</sup>C speed mode is selected to **High Speed Mode**.

## 5. Software electrical validation interface:



## 6. Software electrical validation control panel:



### A. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

### B. Information:

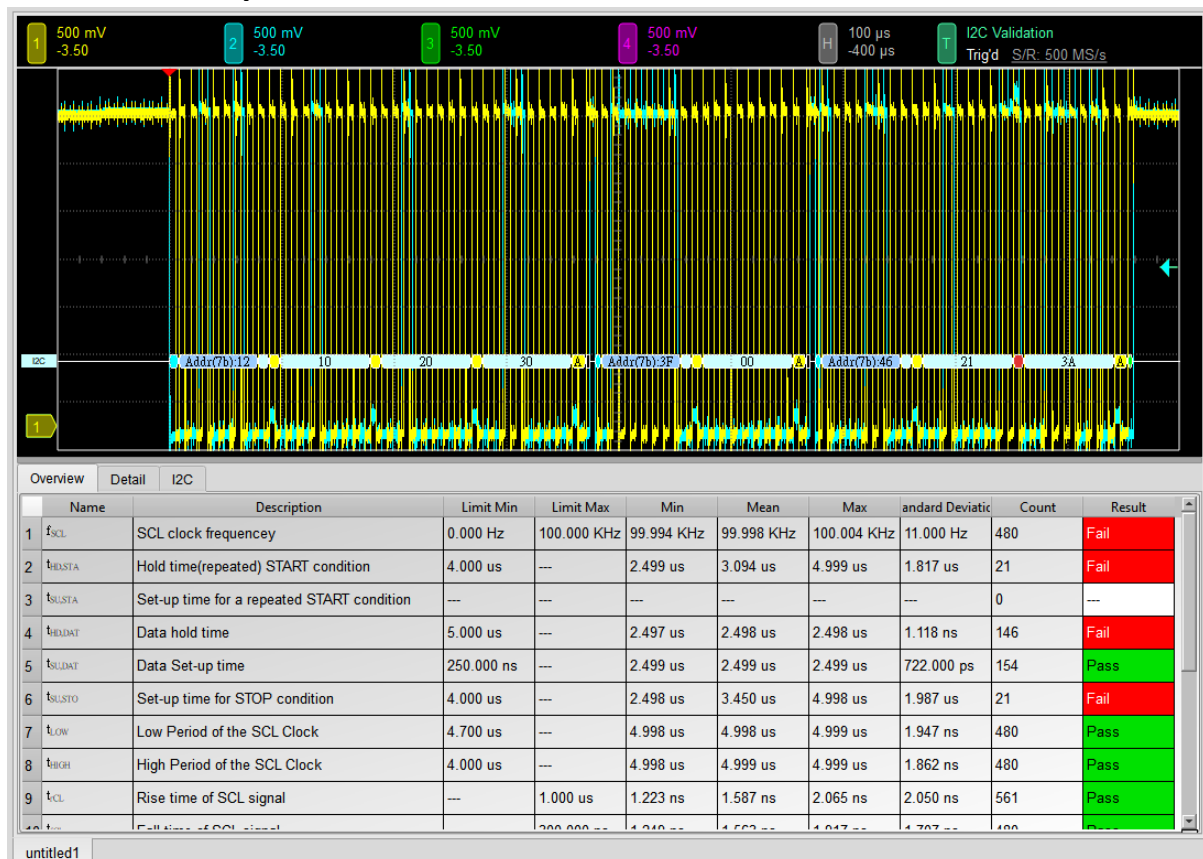
Select waveform

### C. Save File:

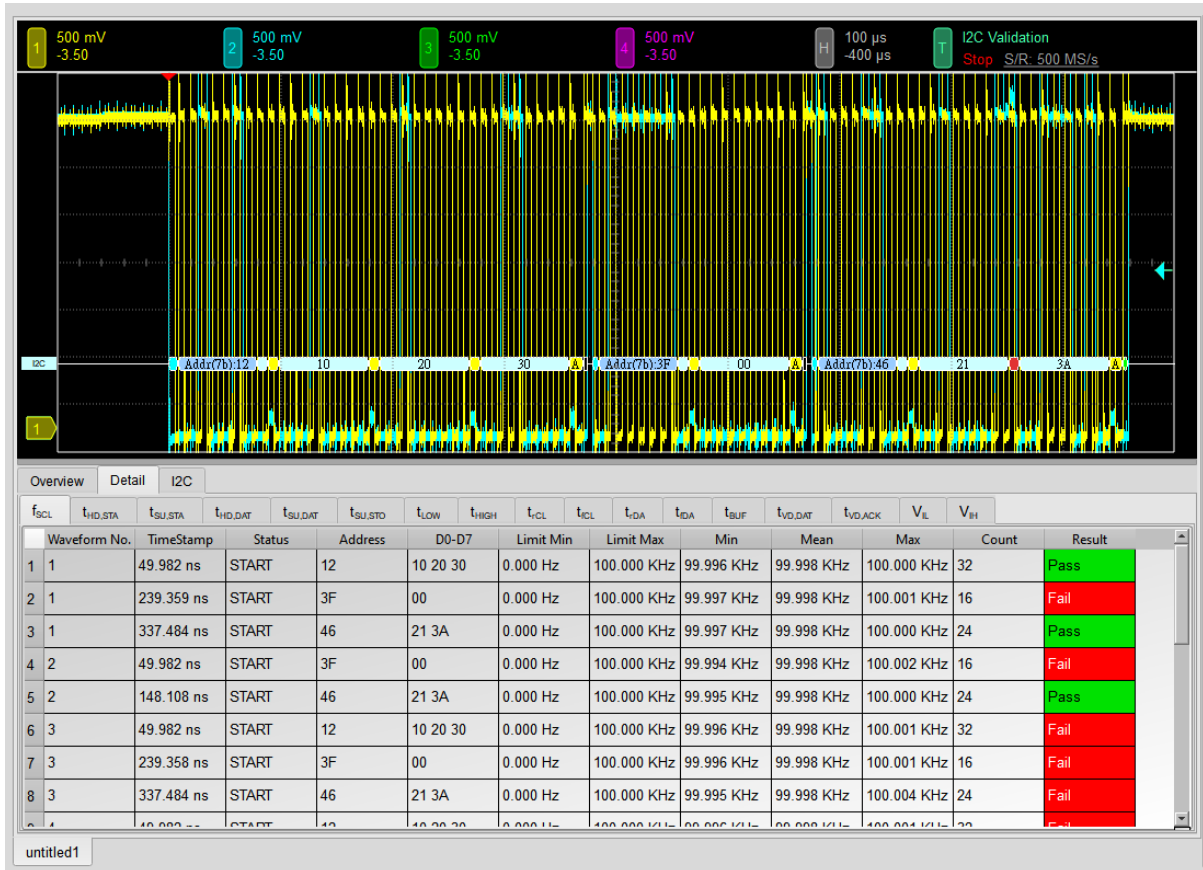
Save as Html

Save as .MOW(Software format)

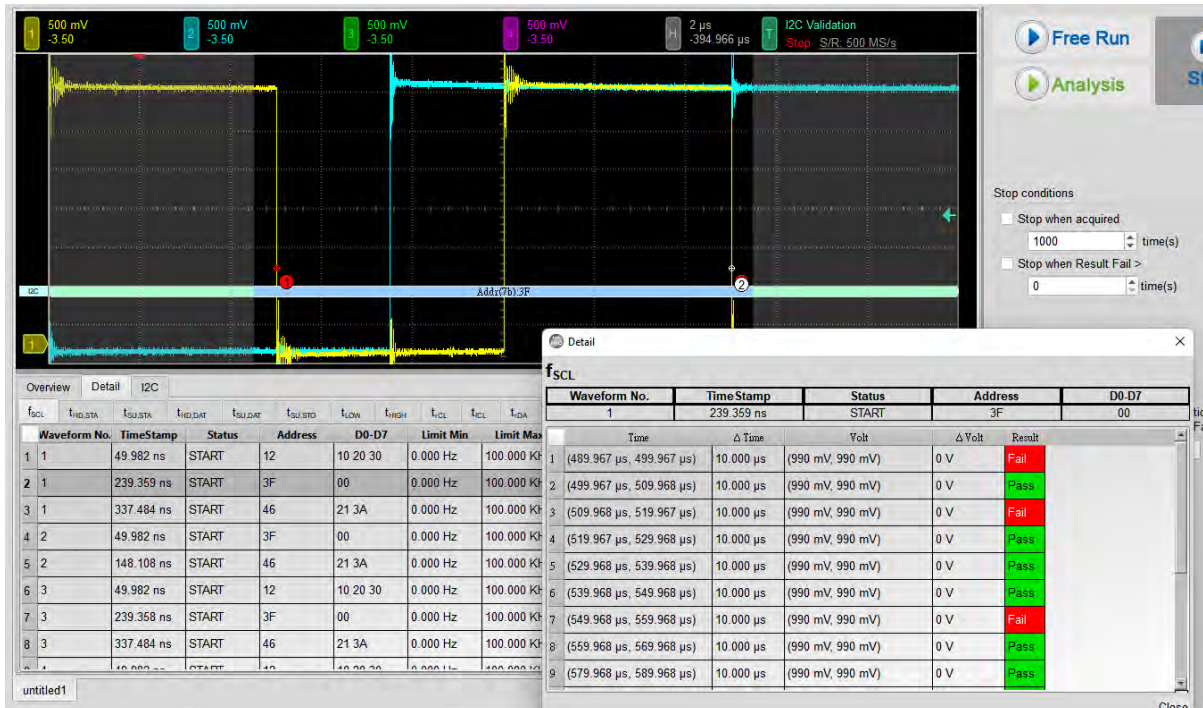
## 7. Overview Report:



## 8. Detail Report:



## 9. Reference Point Dialog & Waveform:



10. **Html Report:**



**Electrical Validation Report**

|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | MSO3124V            |
| Test Instruments Serial Number | 24554               |
| Test Date                      | 04-17-2023 14:46:14 |
| S/W Version                    | 1.0.25              |
| Protocol                       | I2C                 |

```

/*****
DUT INFO
Speed: 400KHz
EEPROM Communication
*****/
    
```

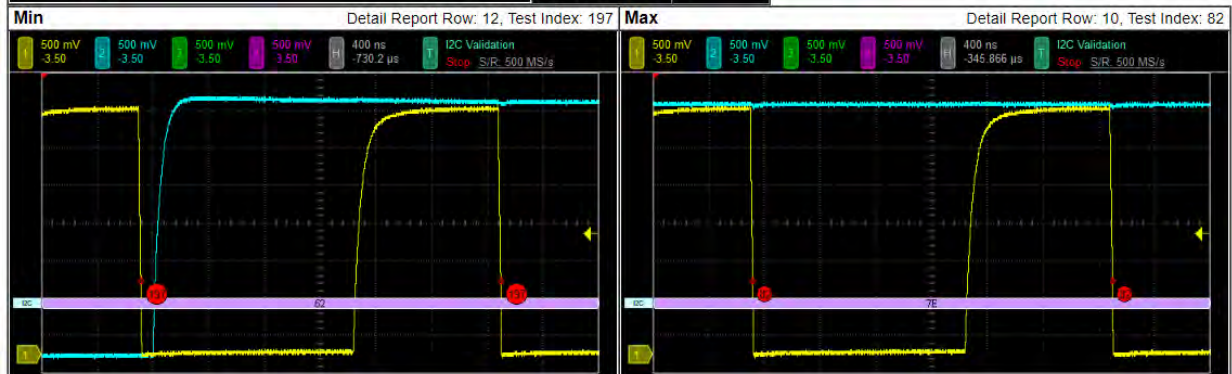
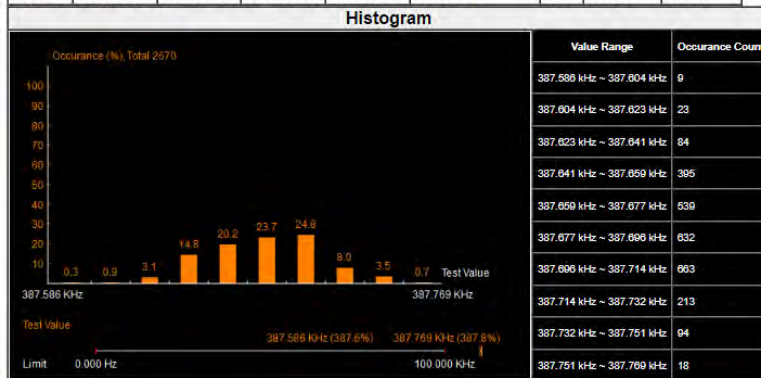
**Overview Results:**

Total: 17  
Pass: 9  
Fail: 6

| Index | Name                | Description                                      | Limit Min   | Limit Max   | Min         | Mean        | Max         | Standard Deviation | Count | Margin Min | Margin Max | Result |
|-------|---------------------|--|-------------|-------------|-------------|-------------|-------------|--------------------|-------|------------|------------|--------|
| 1     | f <sub>SCL</sub>    | SCL clock frequency                              | 0.000 Hz    | 100.000 KHz | 387.586 KHz | 387.683 KHz | 387.769 KHz | 437.000 Hz         | 2670  | 387.6%     | 387.8%     | ✗Fail  |
| 2     | t <sub>HD,STA</sub> | Hold time(repeated) START condition              | 4.000 us    | ---         | 1.538 us    | 1.538 us    | 1.539 us    | 427.000 ps         | 20    | -61.6%     | ---        | ✗Fail  |
| 3     | t <sub>SU,STA</sub> | Set-up time for a repeated START condition       | 4.700 us    | ---         | 2.013 us    | 2.014 us    | 2.015 us    | 579.000 ps         | 10    | -57.2%     | ---        | ✗Fail  |
| 4     | t <sub>HD,DAT</sub> | Data hold time                                   | 5.000 us    | ---         | 94.249 ns   | 247.342 ns  | 1.026 us    | 4.244 us           | 1575  | -98.1%     | ---        | ✗Fail  |
| 5     | t <sub>SU,DAT</sub> | Data Set-up time                                 | 250.000 ns  | ---         | 472.837 ns  | 1.187 us    | 1.443 us    | 5.255 us           | 1767  | 18.7%      | ---        | ✓Pass  |
| 6     | t <sub>SU,STO</sub> | Set-up time for STOP condition                   | ---         | ---         | ---         | ---         | ---         | ---                | 0     | ---        | ---        | ---    |
| 7     | t <sub>LOW</sub>    | Low Period of the SCL Clock                      | 4.700 us    | ---         | 1.539 us    | 1.541 us    | 1.543 us    | 9.208 ns           | 2670  | -67.3%     | ---        | ✗Fail  |
| 8     | t <sub>HIGH</sub>   | High Period of the SCL Clock                     | 4.000 us    | ---         | 977.699 ns  | 979.666 ns  | 984.826 ns  | 20.914 ns          | 3040  | -75.6%     | ---        | ✗Fail  |
| 9     | t <sub>rCL</sub>    | Rise time of SCL signal                          | ---         | 1.000 us    | 45.022 ns   | 48.118 ns   | 49.835 ns   | 14.531 ns          | 3430  | ---        | 0.5%       | ✓Pass  |
| 10    | t <sub>fCL</sub>    | Fall time of SCL signal                          | ---         | 300.000 ns  | 9.888 ns    | 10.237 ns   | 10.583 ns   | 1.448 ns           | 3430  | ---        | 0.2%       | ✓Pass  |
| 11    | t <sub>rDA</sub>    | Rise time of SDA signal                          | ---         | 1.000 us    | 37.719 ns   | 39.529 ns   | 41.848 ns   | 5.148 ns           | 927   | ---        | 0.4%       | ✓Pass  |
| 12    | t <sub>fDA</sub>    | Fall time of SDA signal                          | ---         | 300.000 ns  | 4.616 ns    | 6.893 ns    | 9.828 ns    | 24.035 ns          | 947   | ---        | 1.8%       | ✓Pass  |
| 13    | t <sub>BUF</sub>    | Bus free time between a STOP and START condition | ---         | ---         | ---         | ---         | ---         | ---                | 0     | ---        | ---        | ---    |
| 14    | t <sub>VD,DAT</sub> | Data valid time                                  | ---         | 3.450 us    | 98.898 ns   | 270.164 ns  | 1.067 us    | 4.200 us           | 1585  | ---        | 28.9%      | ✓Pass  |
| 15    | t <sub>VD,ACK</sub> | Data valid acknowledge time                      | ---         | 3.450 us    | 141.017 ns  | 730.257 ns  | 1.067 us    | 1.344 us           | 91    | ---        | 28.0%      | ✓Pass  |
| 16    | V <sub>IL</sub>     | Low-level input voltage                          | -500.000 mV | 990.000 mV  | -105.670 mV | 27.063 mV   | 104.081 mV  | 760.863 mV         | 4367  | 26.5%      | 40.5%      | ✓Pass  |
| 17    | V <sub>IH</sub>     | High-level input voltage                         | 2.310 V     | 3.800 V     | 3.225 V     | 3.267 V     | 3.417 V     | 1.250 V            | 4367  | 61.4%      | 74.3%      | ✓Pass  |

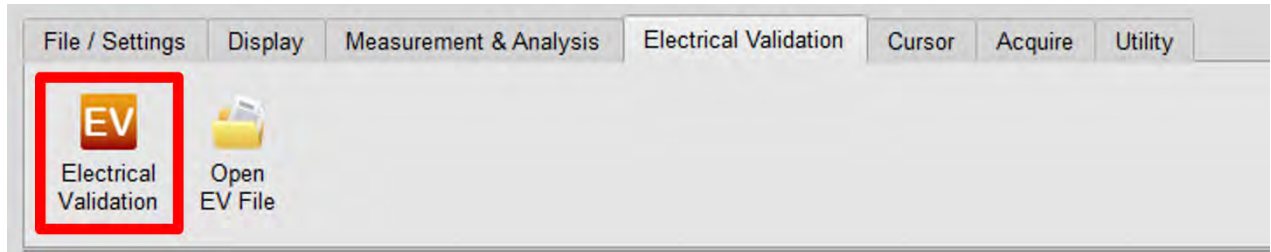
f<sub>SCL</sub> - Test Result: **Fail**  
Description: SCL clock frequency

| Limit Min | Limit Max   | Min         | Mean        | Max         | Standard Deviation | Count | Margin Min | Margin Max |
|-----------|-------------|-------------|-------------|-------------|--------------------|-------|------------|------------|
| 0.000 Hz  | 100.000 KHz | 387.586 KHz | 387.683 KHz | 387.769 KHz | 437.000 Hz         | 2670  | 387.6%     | 387.8%     |



# I2S Electrical Validation Solution

## ■ Introduction:



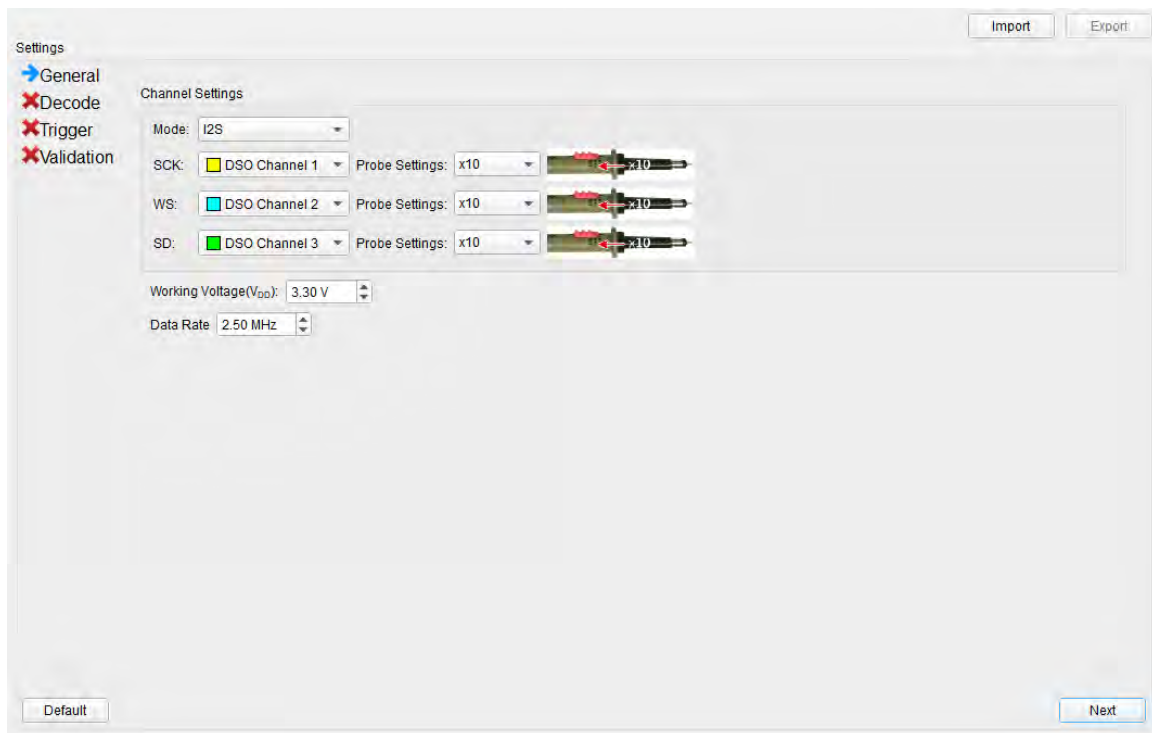
Use an oscilloscope to do I2S Electrical Validation to ensure that the I2S meets the defined specification. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test.

I<sup>2</sup>S (Inter-IC Sound) is a standard electrical serial bus interface used for connecting digital audio devices, such as audio codecs, digital-to-analog converters (DACs), and analog-to-digital converters (ADCs). It is commonly used in embedded systems, audio processors, and high-quality audio equipment.

I<sup>2</sup>S is a straightforward but powerful interface for transmitting digital audio data between devices with high precision and low latency.

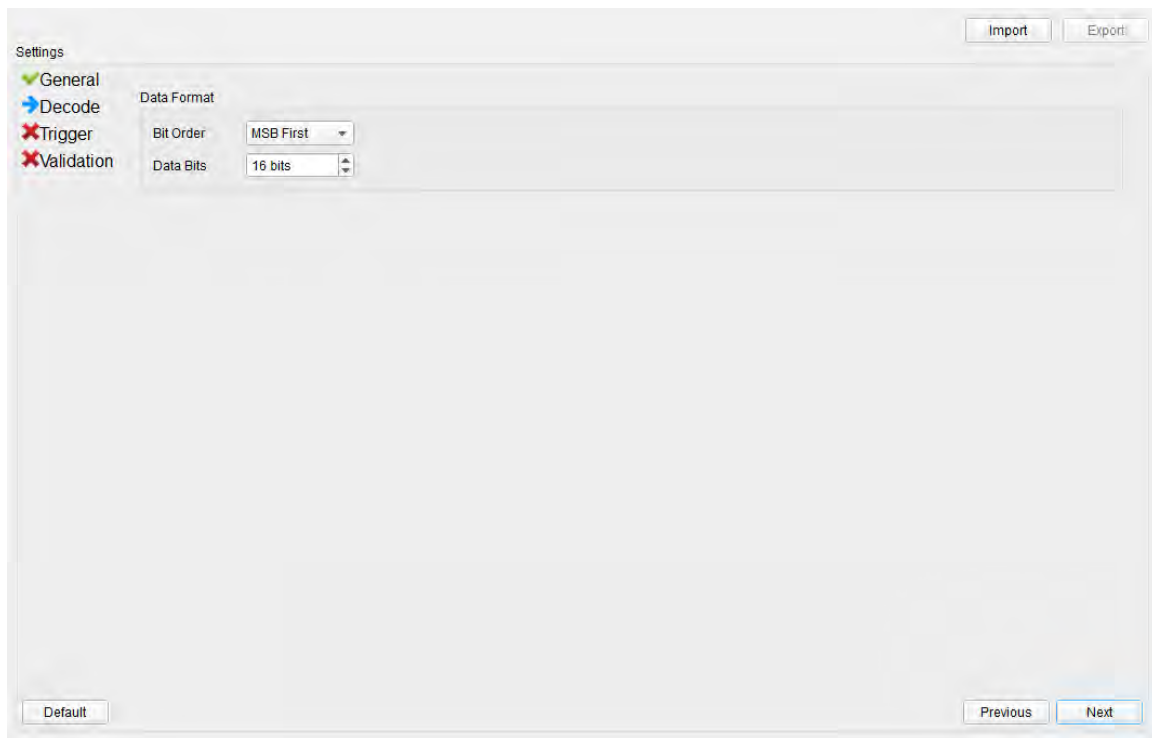
## ■ I2S Electrical Validation Settings:

### 1. General Settings:



In the General Settings section, it is mandatory to setup the bus configuration, including I2S mode type (I2S, Left Justified, PCM, TDM), the channel settings, working voltage and the data rate of I2S.

## 2. Decode Settings:



In the Decode Settings, it requires user to setup the I2S data format. Bit order is either MSB First or LSB First. Data Bits can be set in a range of 1-32 bit(s).

### 3. Trigger Settings:

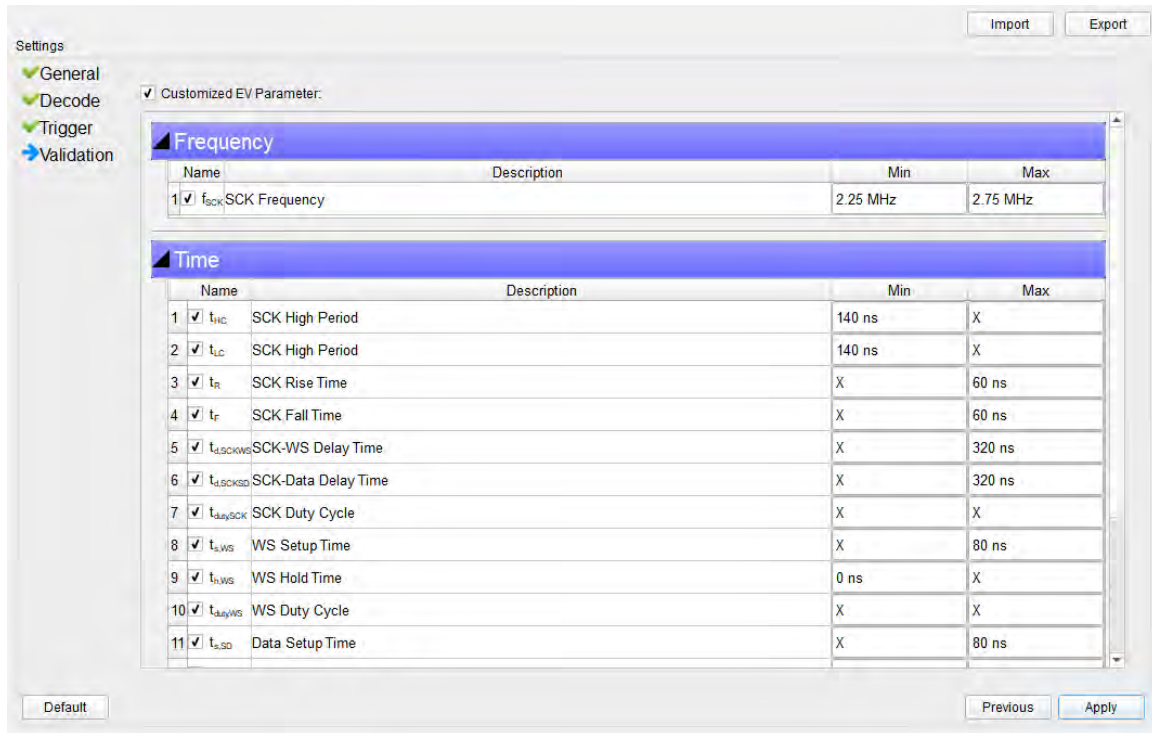
The screenshot shows the 'Settings' dialog box with the 'Trigger' tab selected. The 'Data' section is expanded, showing the following settings:

- Method: Data Match
- Channel: Both
- Pattern: =
- Text field: 0000h
- Duration: 1 frame(s)

Buttons for 'Import', 'Export', 'Default', 'Previous', and 'Next' are visible in the interface.

Set up the data pattern that user expect to trigger on. The data format is set on the previous decode page. The remaining setup is all about the data pattern. Here we provide **Data Match**, **Rising**, **Falling**, **Glitch**, **Mute**, and **Clip**, 6 trigger methods in total.

#### 4. Validation Settings:



This section displays 3 characteristics table, including

1. Frequency
2. Timing Parameters
3. Voltage requirements

The default values are referenced from the I2S specification rev3.0. All supported validation parameters' symbols and description are listed in the table below.

- **I2S Frequency Requirements**

| Symbol    | Electrical Parameter |
|-----------|----------------------|
| $f_{SCK}$ | SCK Clock Frequency  |

- **I2S Timing Requirements**

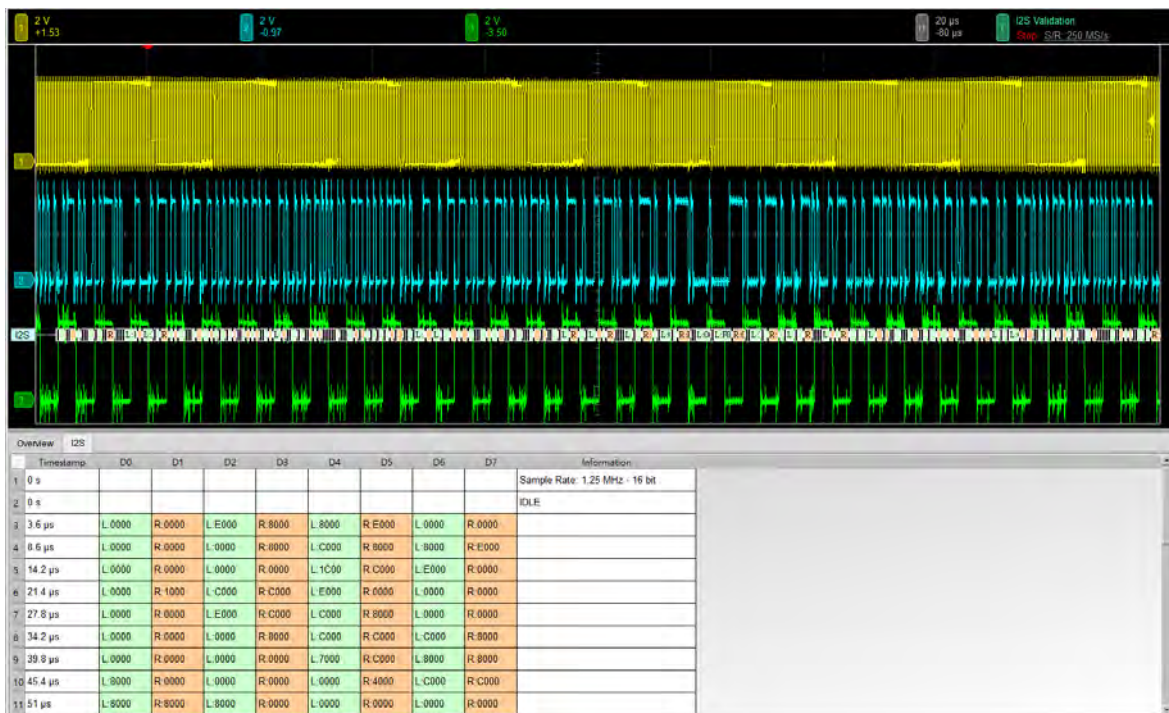
| Symbol        | Electrical Parameter |
|---------------|----------------------|
| $t_{HC}$      | SCK High Period      |
| $t_{LC}$      | SCK Low Period       |
| $t_R$         | SCK Rise Time        |
| $t_F$         | SCK Fall Time        |
| $t_{d,SCKWS}$ | SCK-WS Delay Time    |

|                |                 |
|----------------|-----------------|
| $t_{duty,SCK}$ | SCK Duty Cycle  |
| $t_{s,WS}$     | WS Setup Time   |
| $t_{h,WS}$     | WS Hold Time    |
| $t_{duty,WS}$  | WS Duty Cycle   |
| $t_{s,SD}$     | Data Setup Time |
| $t_{h,SD}$     | Data Hold Time  |

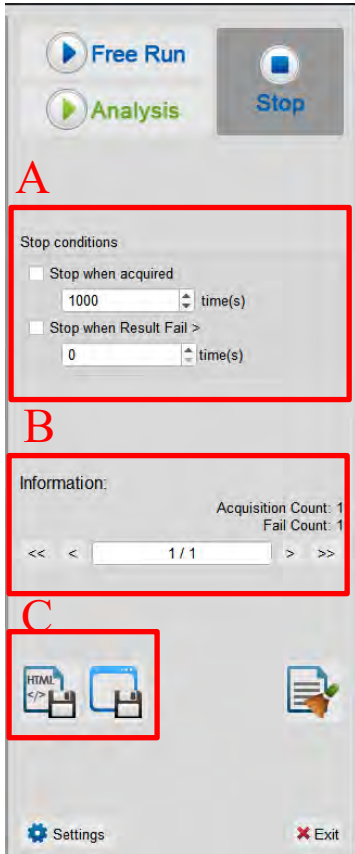
• **I2S Voltage Requirements**

| Symbol | Electrical Parameter |
|--------|----------------------|
| $V_L$  | Low-Level Voltage    |
| $V_H$  | High-level Voltage   |

5. Software electrical validation interface:

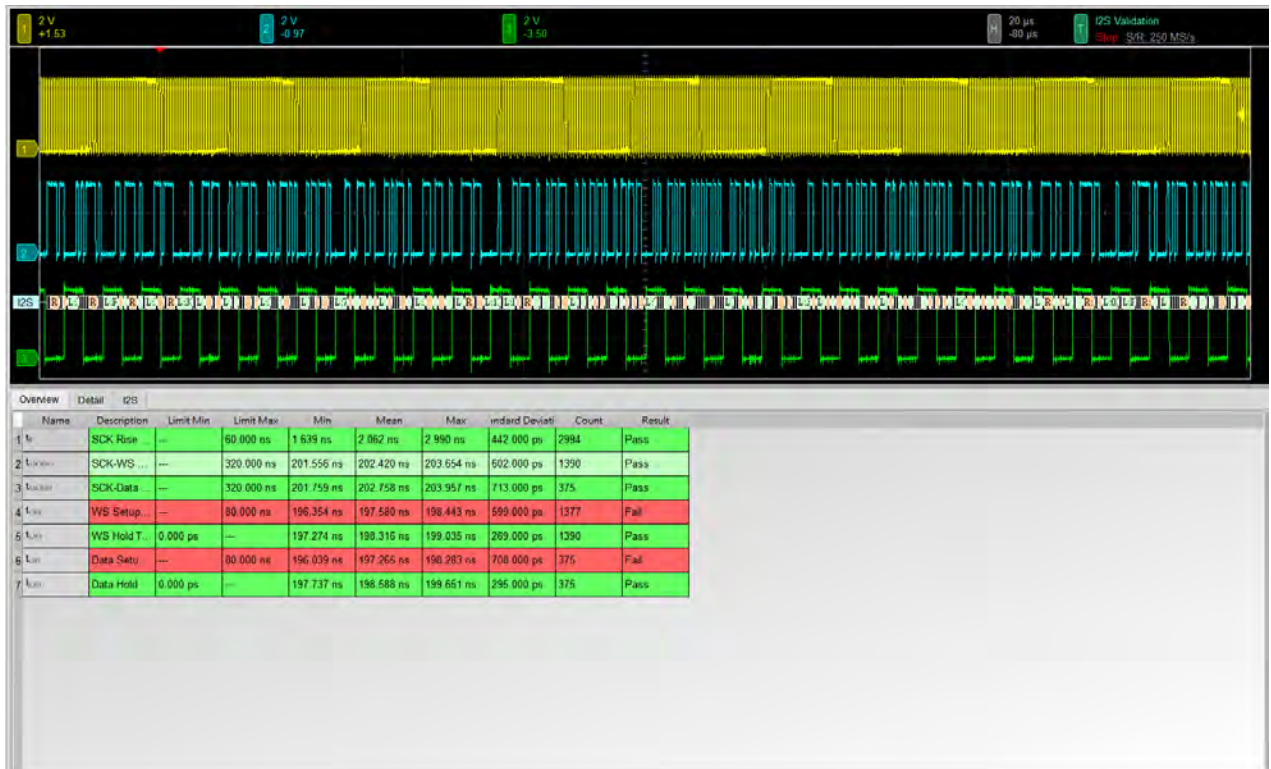


6. Software electrical validation control panel:

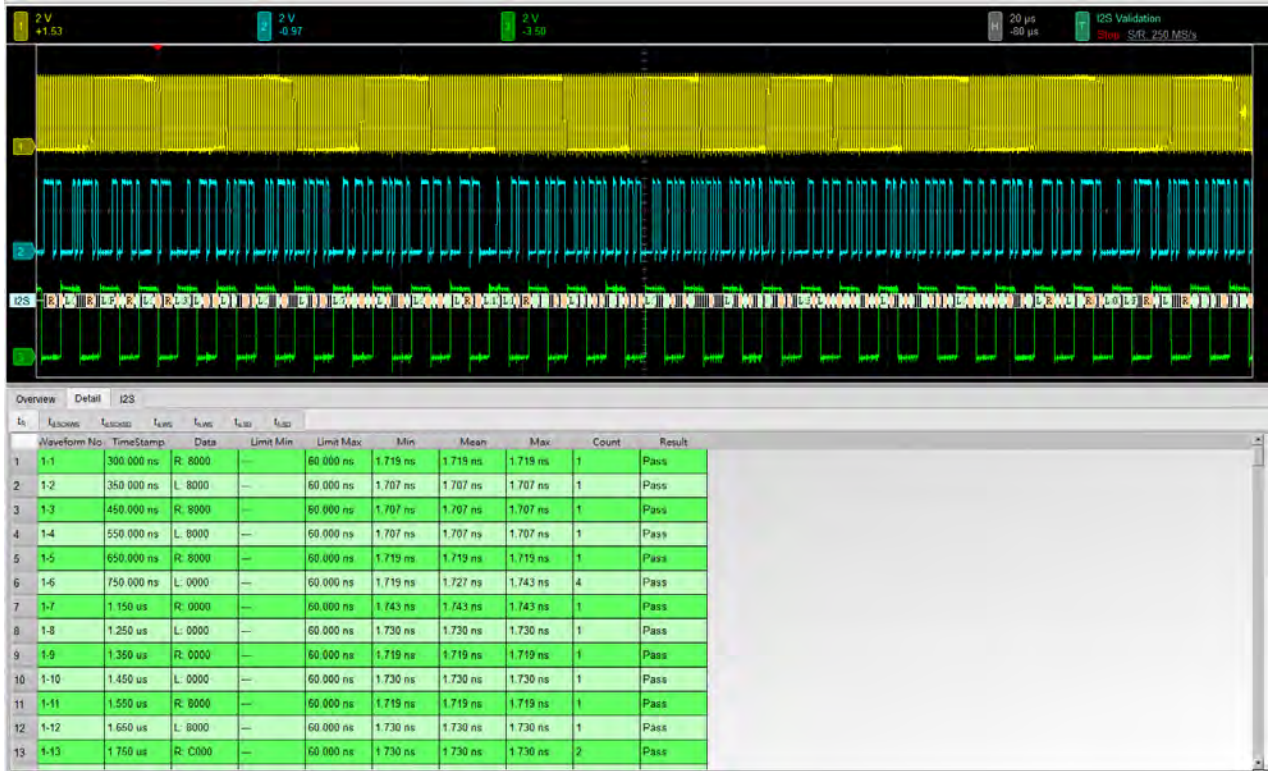


1. **Stop Conditions:**  
Stop when acquired X times  
Stop when Result Fail > X times
2. **Information:**  
Select waveform
3. **Save File:**  
Save as Html  
Save as .MOW(Software format)

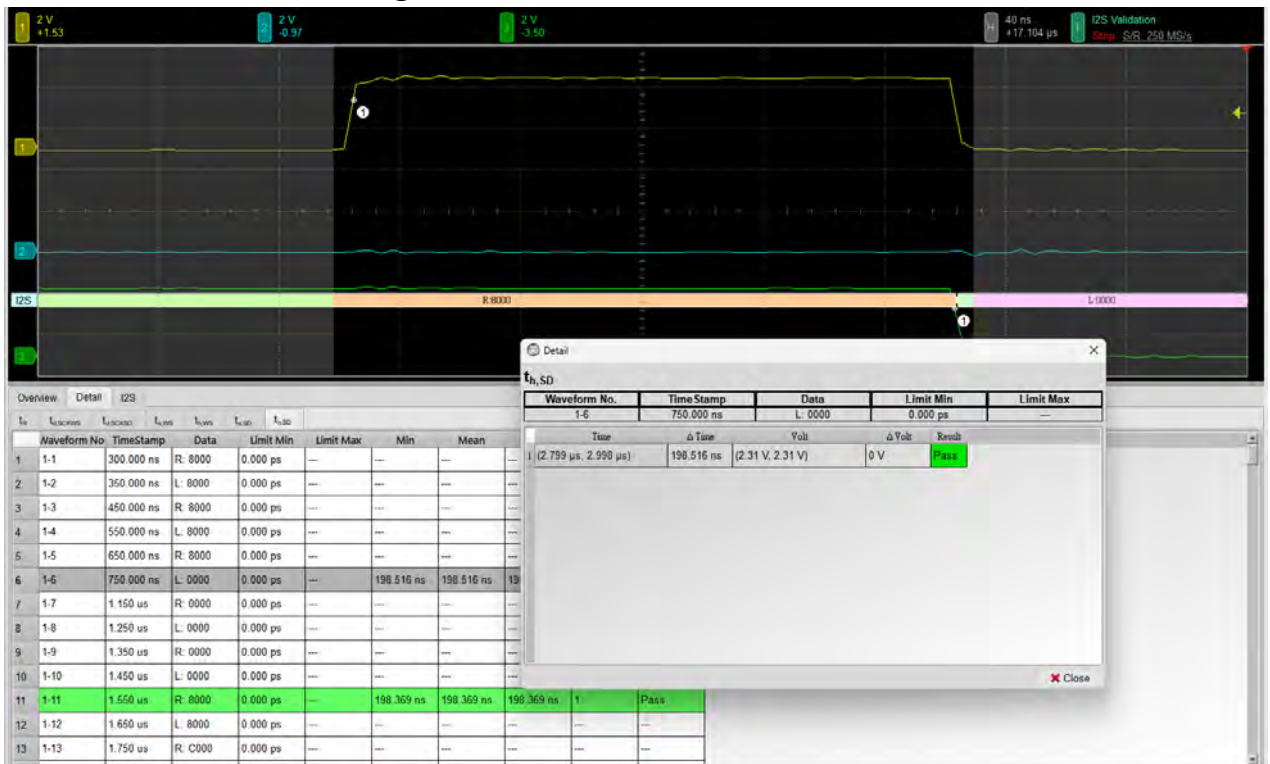
7. Overview Report:



### 8. Detail Report:



### 9. Reference Point Dialog & Waveform:



## 10. Html Report:



### Electrical Validation Report

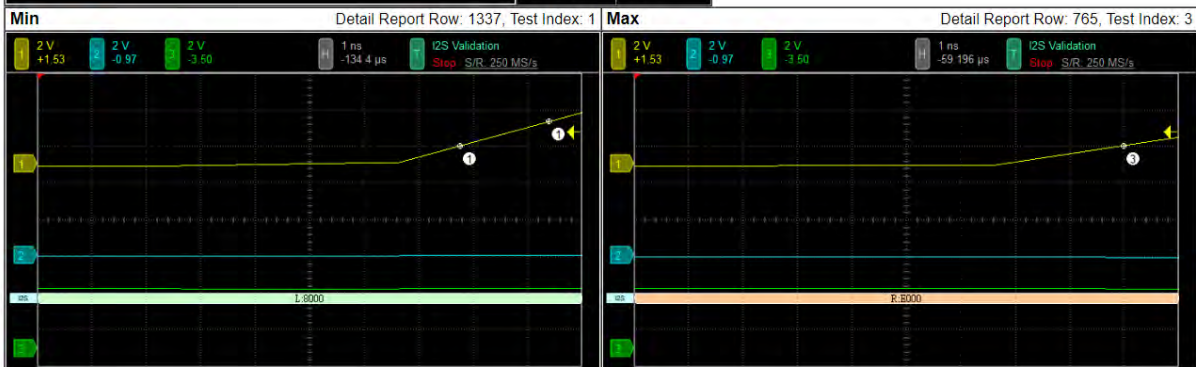
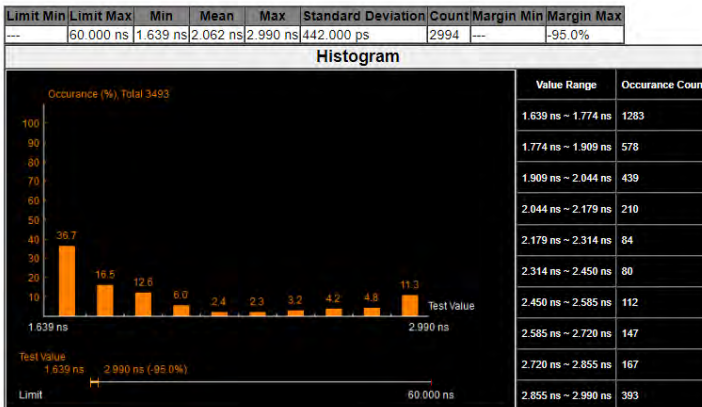
|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | MSO3124V            |
| Test Instruments Serial Number | MSV31240021         |
| Test Date                      | 12-09-2024 13:34:37 |
| S/W Version                    | 1.8.62              |
| Protocol                       | I2S                 |

#### Overview Results:

Total: 7  
Pass: 5  
Fail: 2

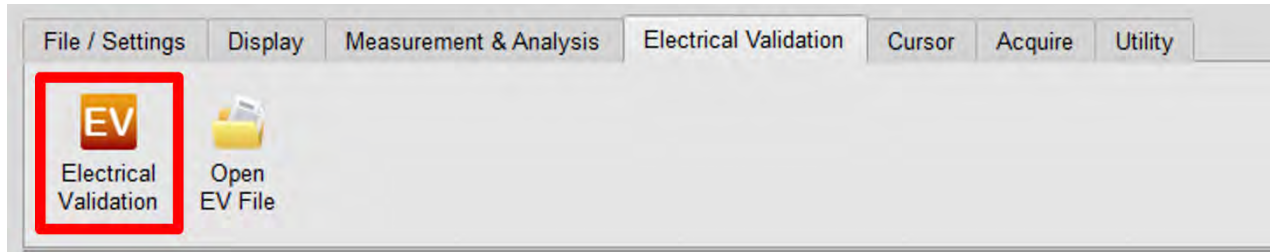
| Index | Name                 | Description                         | Limit Min | Limit Max  | Min        | Mean       | Max        | Standard Deviation | Count | Margin Min | Margin Max | Result |
|-------|----------------------|-------------------------------------|-----------|------------|------------|------------|------------|--------------------|-------|------------|------------|--------|
| 1     | t <sub>R</sub>       | <a href="#">SCK Rise Time</a>       | ---       | 60.000 ns  | 1.639 ns   | 2.062 ns   | 2.990 ns   | 442.000 ps         | 2994  | ---        | -95.0%     | ✓Pass  |
| 2     | t <sub>d,SCKWS</sub> | <a href="#">SCK-WS Delay Time</a>   | ---       | 320.000 ns | 201.556 ns | 202.420 ns | 203.654 ns | 602.000 ps         | 1390  | ---        | -36.4%     | ✓Pass  |
| 3     | t <sub>d,SCKSD</sub> | <a href="#">SCK-Data Delay Time</a> | ---       | 320.000 ns | 201.759 ns | 202.758 ns | 203.957 ns | 713.000 ps         | 375   | ---        | -36.3%     | ✓Pass  |
| 4     | t <sub>s,WS</sub>    | <a href="#">WS Setup Time</a>       | ---       | 80.000 ns  | 196.354 ns | 197.580 ns | 198.443 ns | 599.000 ps         | 1377  | ---        | 148.1%     | ✗Fail  |
| 5     | t <sub>h,WS</sub>    | <a href="#">WS Hold Time</a>        | 0.000 ps  | ---        | 197.274 ns | 198.316 ns | 199.035 ns | 269.000 ps         | 1390  | ---        | ---        | ✓Pass  |
| 6     | t <sub>s,SD</sub>    | <a href="#">Data Setup Time</a>     | ---       | 80.000 ns  | 196.039 ns | 197.265 ns | 198.283 ns | 708.000 ps         | 375   | ---        | 147.9%     | ✗Fail  |
| 7     | t <sub>h,SD</sub>    | <a href="#">Data Hold Time</a>      | 0.000 ps  | ---        | 197.737 ns | 198.588 ns | 199.651 ns | 295.000 ps         | 375   | ---        | ---        | ✓Pass  |

t<sub>R</sub> - Test Result: **Pass**  
Description: SCK Rise Time



# MIPI I3C Electrical Validation Solution

## ■ Introduction:



MIPI I3C is backward compatible with many Legacy I<sup>2</sup>C Devices, but I3C Devices also support higher speed (with SCL clock speed up to 12.5 MHz) and new communication modes. MIPI I3C modes include **Single Data Rate (SDR) Mode**, **High Data Rate (HDR) Mode**. HDR Mode is also divided into **Dual Data Rate (HDR-DDR) Mode**, **Ternary Symbol Legacy Mode (HDR-TTL) Mode**, **Ternary Symbol Pure-bus (HDR-TSP) Mode**, and **Bulk Transport (HDR-BT) Mode**.

MIPI I3C Electrical Validation offers various electrical measurements compliance testing as specified in the MIPI I3C Specification (currently supports MIPI I3C version 1.1.1).

## ■ MIPI I3C Electrical Validation Settings:

### 1. General Settings: Channel sources, working voltage and speed

Settings

Import Export

General  
Decode  
Trigger  
Validation

Channel Settings

SCL: DSO Channel 1 Probe Settings: x10

SDA: DSO Channel 2 Probe Settings: x10

Working Voltage( $V_{DD}$ ): 1.80 V

Speed Mode

- SDR: Single Data Rate Mode (Max: 12.5 Mbps)
- HDR-DDR: HDR Double Data Rate Mode (Max: 25 Mbps)
- HDR-TSL: Tenary Symbol Legacy-inclusive-bus Mode (Max: 27.5 Mbps)
- HDR-TSP: HDR Tenary Symbol for Pure-bus Mode (Max: 39.5 Mbps)
- HDR-BT: HDR Bulk Transport Mode
- Customized Speed 400 Kbps

Bus Configuration

- Pure Bus: Only I3C devices are presented on the I3C Bus
- Mixed Bus: At least one I2C Legacy Device is presented on the I3C Bus

Communicating with I2C Legacy Device

- Fast Mode (400 Kbps)
- Fast Mode+ (1 Mbps)

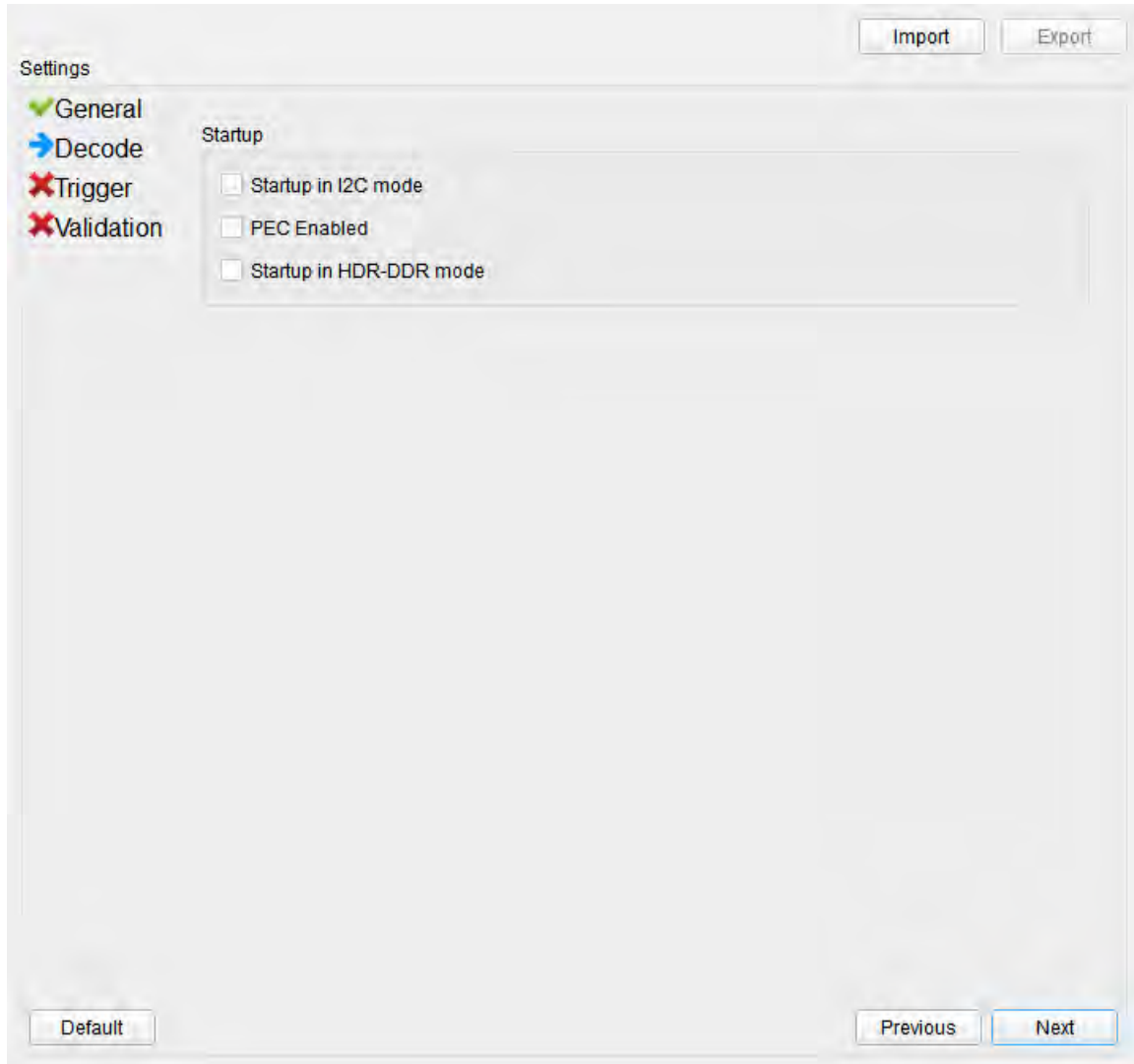
Default Next

In the General Settings section, the selection of Speed Mode determines a suitable sample rate for validation, but also affects the timing specification table in the validation settings section. For instance, in HDR-TSL and HDR-TSP Mode, there are additional timing specifications listed in the table.

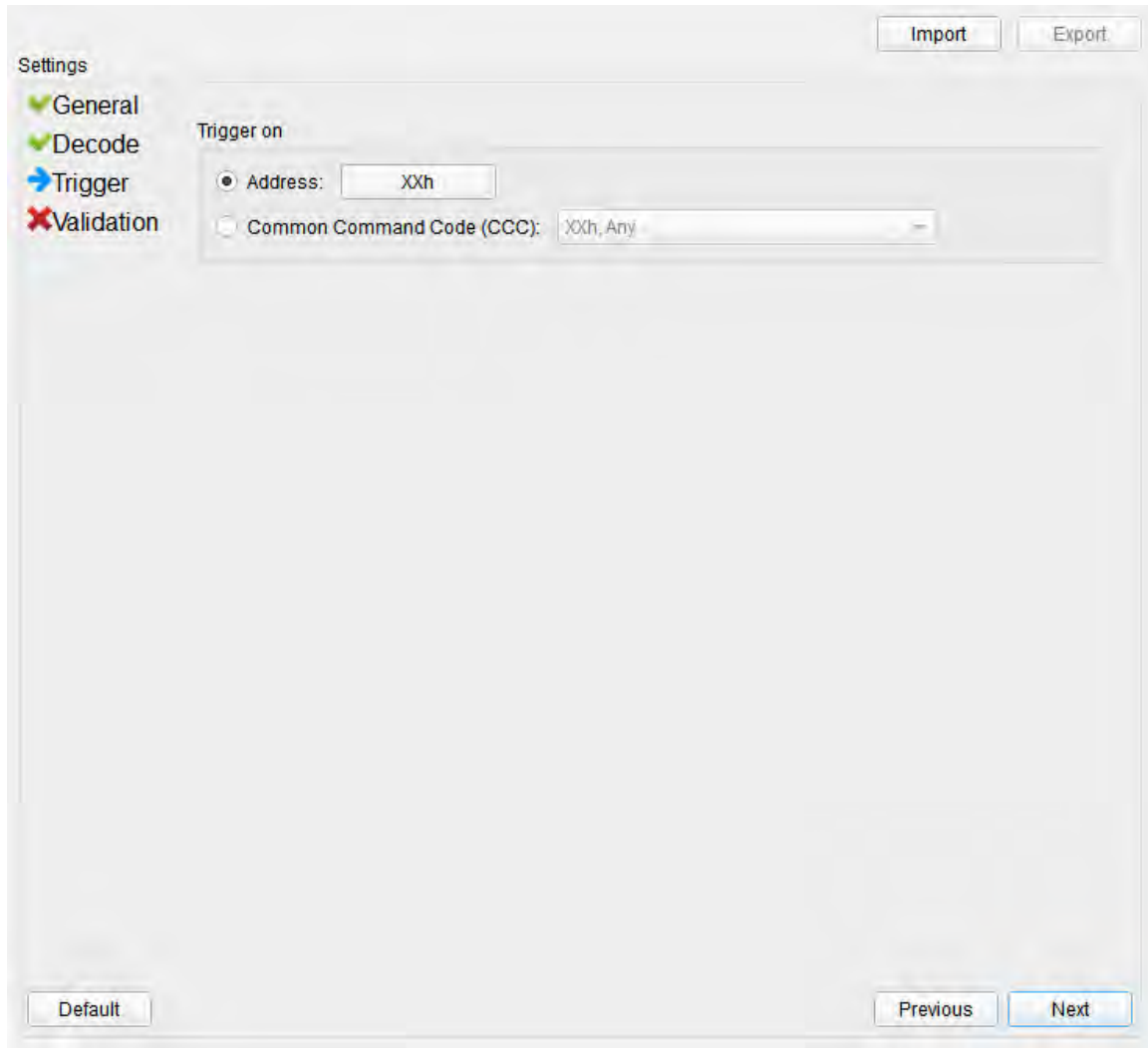
|    |                                     |              |  |         |         |
|----|-------------------------------------|--------------|--|---------|---------|
| 13 | <input checked="" type="checkbox"/> | $t_{EDGE}$   | Edge-to-Edge Period  | 32 ns   | X       |
| 14 | <input checked="" type="checkbox"/> | $t_{SKEW}$   | Allow Difference Between Signals for 'Simultaneous' Change | X       | 12.8 ns |
| 15 | <input checked="" type="checkbox"/> | $t_{EYE}$    | Stable Condition Between Signals                           | 12 ns   | X       |
| 16 | <input checked="" type="checkbox"/> | $t_{SYMBOL}$ | Time Between Successive Symbols                            | 32 ns   | X       |
| 17 | <input checked="" type="checkbox"/> | $t_{CLOCK}$  | Symbol Clock   | 77.5 ns | X       |

Furthermore, the Bus Configuration section specifies the devices you connected on the I3C Bus. If it is a Pure-Bus setup, I<sup>2</sup>C timing table is thus not required, which is discussed in the Validation Settings section. On the other hand, a Mixed Bus setup will include the timing table for I<sup>2</sup>C Legacy Devices, and their default timing values are determined by using Fast Mode (Fm) or Fast Mode (Fm+) configuration, which is an identical settings to I<sup>2</sup>C Electrical Validation setup.

## 2. Decode Settings



### 3. Trigger Settings



If you are interested in analyzing specific devices address, set the trigger address to the value you prefer. In the figure above, “XX” stands for don’t care term. Thus, it triggers on all address in this case. It also provides triggering on Common Command Code (CCC), which is specified on the Broadcast Address 7’h7E.

## 4. Validation Settings

Settings Import Export

General  
 Decode  
 Trigger  
 Validation

Customized EV Parameter:

| Frequency |   |  |          |          |
|-----------|---|--|----------|----------|
|           | Name  | Description  | Min      | Max      |
| 1         | <input checked="" type="checkbox"/> f <sub>SCL</sub>    | SCL Clock Frequency when communicating with I2C Legacy Devices | 0 MHz    | 0.4 MHz  |
| 2         | <input checked="" type="checkbox"/> f <sub>SCL_PP</sub> | SCL Clock Frequency  | 0.01 MHz | 12.9 MHz |

| Time (When Communicating With I2C Legacy Devices) |   |   |           |        |
|---|---|---|-----------|--------|
|   | Name  | Description                                   | Min       | Max    |
| 1   | <input checked="" type="checkbox"/> t <sub>SU_STA</sub> | Setup Time for a Repeated START               | 600 ns    | X      |
| 2   | <input checked="" type="checkbox"/> t <sub>HD_STA</sub> | Hold Time for a (Repeated) START              | 600 ns    | X      |
| 3   | <input checked="" type="checkbox"/> t <sub>LOW</sub>    | SCL Clock Low Period                          | 1300 ns   | X      |
| 4   | <input checked="" type="checkbox"/> t <sub>DIG_L</sub>  | SCL Clock Low Period as seen at the receiver  | 1320 ns   | X      |
| 5   | <input checked="" type="checkbox"/> t <sub>HIGH</sub>   | SCL Clock High Period                         | 600 ns    | X      |
| 6   | <input checked="" type="checkbox"/> t <sub>DIG_H</sub>  | SCL Clock High Period as seen at the receiver | 606.55 ns | X      |
| 7   | <input checked="" type="checkbox"/> t <sub>SU_DAT</sub> | Data Setup Time                               | 100 ns    | X      |
| 8   | <input checked="" type="checkbox"/> t <sub>HD_DAT</sub> | Data Hold Time                                | X         | X      |
| 9   | <input checked="" type="checkbox"/> t <sub>CL</sub>     | SCL Signal Rise Time                          | 20 ns     | 300 ns |
| 10  | <input checked="" type="checkbox"/> t <sub>FL</sub>     | SCL Signal Fall Time                          | 6.55 ns   | 300 ns |

Default Previous Apply

This section includes 5 parameter tables, including

- Frequency
- I3C timing requirements when communicating with I<sup>2</sup>C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

All specification table are listed below.

In the Pure Bus setup, the timing requirements table with I<sup>2</sup>C Legacy Devices is not required and thus be hidden from the parameter settings dialog. The frequency parameter f<sub>SCL</sub> will also be hidden in the Pure Bus setup.

### MIPI I3C Frequency Requirements

| Symbol         | Electrical Parameter   |
|----------------|--|
| $f_{SCL}$      | SCL Clock Frequency when communicating with I <sup>2</sup> C Legacy Devices <sup>1</sup> |
| $t_{SCL\_PP}$  | SCL Clock Frequency  |
| $t_{BT\_FREQ}$ | HDR-BT SCL Clock Frequency   |

### MIPI I3C Timing Requirements When Communicating With I<sup>2</sup>C Legacy Devices<sup>1</sup>

| Symbol        | Electrical Parameter                                  |
|---------------|---|
| $t_{SU\_STA}$ | Setup Time for a REPEATED START                       |
| $t_{HD\_STA}$ | Hold Time for a (REPEATED) START                      |
| $t_{LOW}$     | SCL Clock Low Period                                  |
| $t_{DIG\_L}$  | SCL Clock Low Period as seen at the receiver          |
| $t_{HIGH}$    | SCL Clock High Period                                 |
| $t_{DIG\_H}$  | SCL Clock High Period as seen at the receiver         |
| $t_{SU\_DAT}$ | Data Setup Time                                       |
| $t_{HD\_DAT}$ | Data Hold Time  |
| $t_{rCL}$     | SCL Signal Rise Time                                  |
| $t_{fCL}$     | SCL Signal Fall Time                                  |
| $t_{rDA}$     | SDA Signal Rise Time                                  |
| $t_{rDA\_OD}$ | SDA Signal Rise Time (Open Drain)                     |
| $t_{fDA}$     | SDA Signal Fall Time                                  |
| $t_{SU\_STO}$ | Setup Time for STOP                                   |
| $t_{BUF}$     | Bus Free Time Between a STOP and a START              |
| $t_{SPIKE}$   | Pulse Width of Spikes that Spike Filter Must Suppress |

<sup>1</sup> Only available when the bus configuration is set to Mixed Bus (i.e. at least one I<sup>2</sup>C legacy device is presented on the I3C bus).

### MIPI I3C Open Drain Timing Requirements

| Symbol            | Electrical Parameter                                       |
|-------------------|--|
| $t_{LOW\_OD}$     | SCL Clock Low Period                                       |
| $t_{DIG\_OD\_L}$  | SCL Clock Low Period as seen at the receiver               |
| $t_{HIGH\_INIT}$  | High Period of SCL Clock (for First Broadcast Address)     |
| $t_{HIGH\_OD}$    | SCL Clock High Period                                      |
| $t_{DIG\_OD\_H}$  | SCL Clock High Period as seen at the receiver              |
| $t_{fDA\_OD}$     | SDA Data Fall Time   |
| $t_{SU\_OD}$      | SDA Data Setup Time During Open Drain Mode                 |
| $t_{CAS}$         | Clock After START (S) Condition                            |
| $t_{CBP}$         | Clock Before STOP (P) Condition                            |
| $t_{CRHPOverlap}$ | Active Controller to Secondary Overlap time during handoff |
| $t_{AVAL}$        | Bus Available Condition                                    |
| $t_{IDLE}$        | Bus Idle Condition   |
| $t_{NEWCRlock}$   | Time Interval Where New Controller Not Driving SDA Low     |

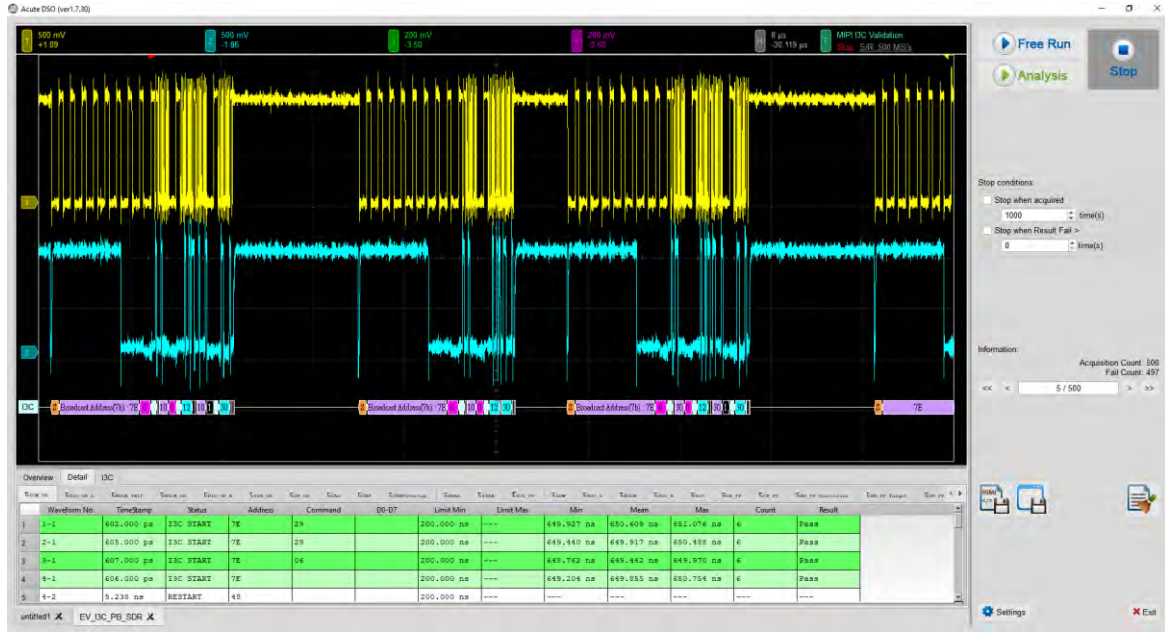
### MIPI I3C Push-Pull Timing Requirements

| Symbol                   | Electrical Parameter                          |
|--------------------------|---|
| $t_{LOW}$                | SCL Clock Low Period                          |
| $t_{DIG\_L}$             | SCL Clock Low Period as seen at the receiver  |
| $t_{HIGH}$               | SCL Clock High Period                         |
| $t_{DIG\_H}$             | SCL Clock High Period as seen at the receiver |
| $t_{SCO}$                | Clock in to Data Out for Target               |
| $t_{CR\_PP}$             | SCL Clock Rise Time                           |
| $t_{CF\_PP}$             | SCL Clock Fall Time                           |
| $t_{HD\_PP\_Controller}$ | SDA Signal Data Hold (Controller)             |
| $t_{HD\_PP\_Target}$     | SDA Signal Data Hold (Target)                 |
| $t_{SU\_PP}$             | SDA Signal Data Setup                         |
| $t_{CASr}$               | Clock After Repeated START (Sr) Condition     |
| $t_{CBSr}$               | Clock Before Repeated START (Sr) Condition    |
| $t_{BT\_HO}$             | HDR-BT Master to Slave Hand Off Delay         |
| $t_{BT\_STALL}$          | HDR-BT Clocked Not-Ready Data-Block Headers   |

### MIPI I3C I/O Stage Characteristics Voltage Requirements

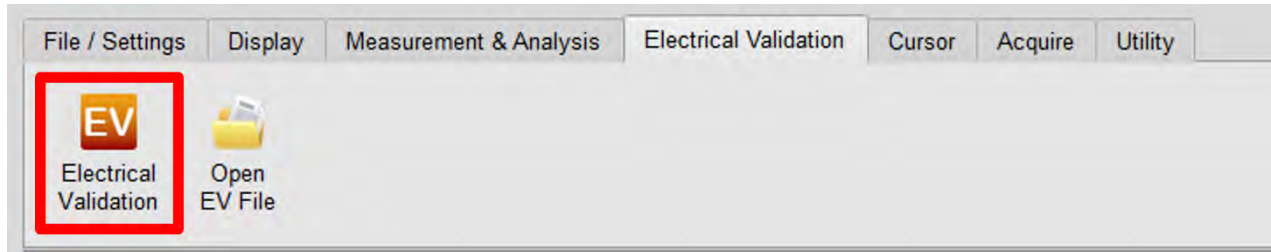
| Symbol          | Electrical Parameter      |
|-----------------|---------------------------|
| V <sub>IL</sub> | Low-Level Input Voltage   |
| V <sub>IH</sub> | High-level Input Voltage  |
| V <sub>OL</sub> | Low-level Output Voltage  |
| V <sub>OH</sub> | High-level Output Voltage |

## 5. Sample Result



# MIPI RFFE Electrical Validation Solution

## ■ Introduction:

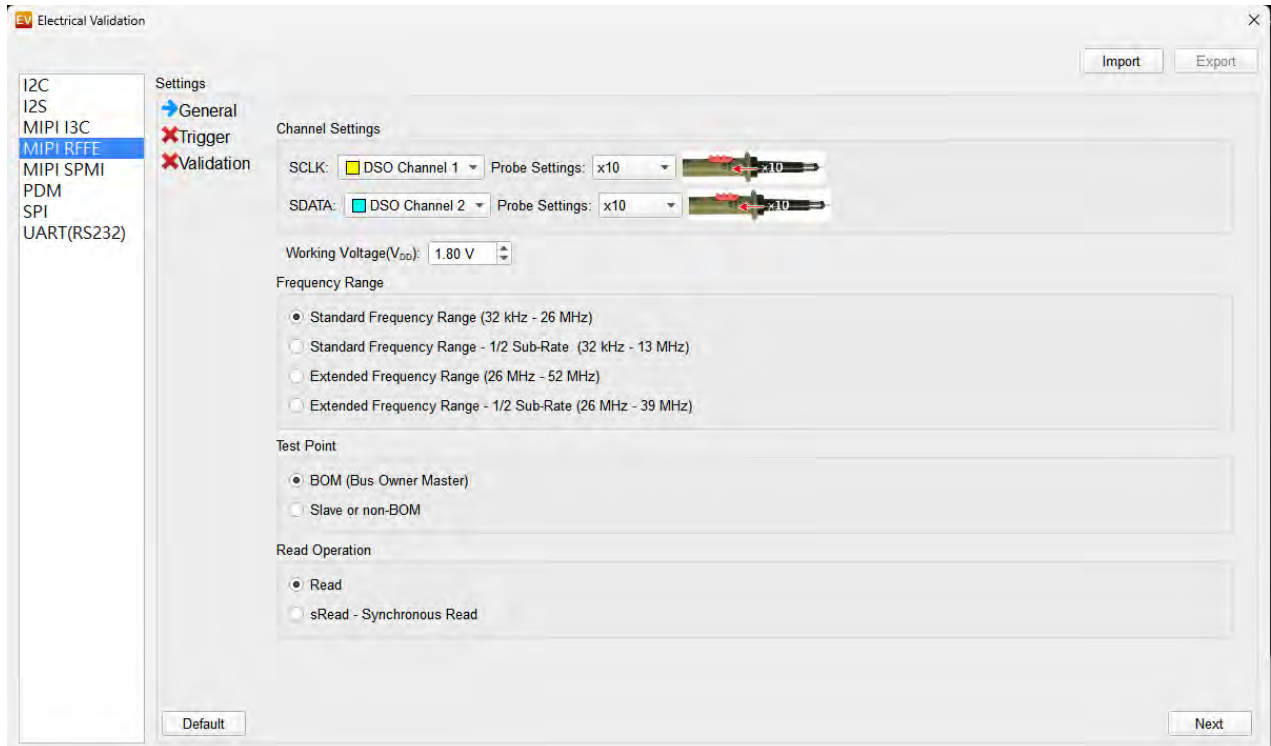


MIPI RFFE (Radio Frequency Front-End) is a standard developed by the MIPI Alliance to define the interface between baseband processors and radio frequency front-end modules in mobile devices, such as smartphones and tablets. It is part of the broader MIPI (Mobile Industry Processor Interface) family, which includes various standards for efficient communication between different components in mobile and embedded devices.

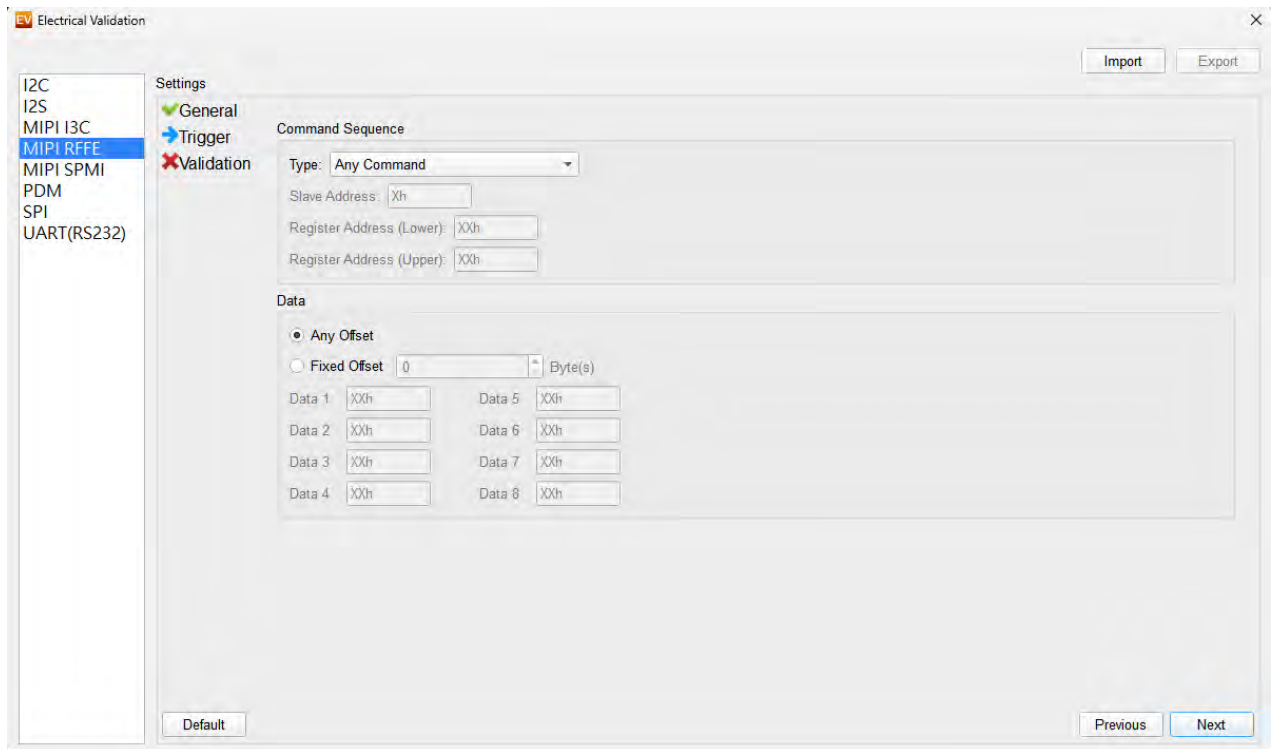
MIPI RFFE is a key enabler in modern wireless devices, providing a standardized and efficient interface for controlling the RF front-end components in mobile and wireless communication systems.

## MIPI RFFE Electrical Validation Settings:

### 1. General Settings: Channel sources, Working Voltage, Frequency Range, Test Point and Read Operation



### 2. Trigger Settings:



### 3. Electrical Validation: Voltage, Timing and Frequency limitation

The screenshot shows the 'Electrical Validation' window with the following settings:

- Settings:** General, Trigger, Validation
- Customized EV Parameter:**
  - Frequency:**

| Name | Description                      | Min       | Max    |
|------|----------------------------------|-----------|--------|
| 1    | f <sub>SCLK</sub> SCLK Frequency | 0.032 MHz | 26 MHz |
  - Time (Full-Speed Operations)**
  - Time (Half-Speed Data Response Operations):**

| Name | Description  | Min     | Max    |
|------|--|---------|--------|
| 1    | t <sub>SCLKOH</sub> (HSDR) Clock Output High Time  | 28.1 ns | X      |
| 2    | t <sub>SCLKOL</sub> (HSDR) Clock Output Low Time   | 28.1 ns | X      |
| 3    | t <sub>SCLKOTR</sub> (HSDR) Clock Output Transition (Rise/Fall) Time                     | 3.5 ns  | 6.5 ns |
| 4    | t <sub>SD, M, RD</sub> (HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read | 3.75 ns | X      |
| 5    | t <sub>SD, M, RD</sub> (HSDR) SDATA Hold Time, with respect to SCLK Output - BOM - Read  | 6.75 ns | X      |
  - Voltage:**

| Name | Description                          | Min    | Max    |
|------|--------------------------------------|--------|--------|
| 1    | V <sub>LOW</sub> Low-Level Voltage   | 0 V    | 0.36 V |
| 2    | V <sub>HIGH</sub> High-Level Voltage | 1.44 V | 1.8 V  |

### 4. Software electrical validation interface:

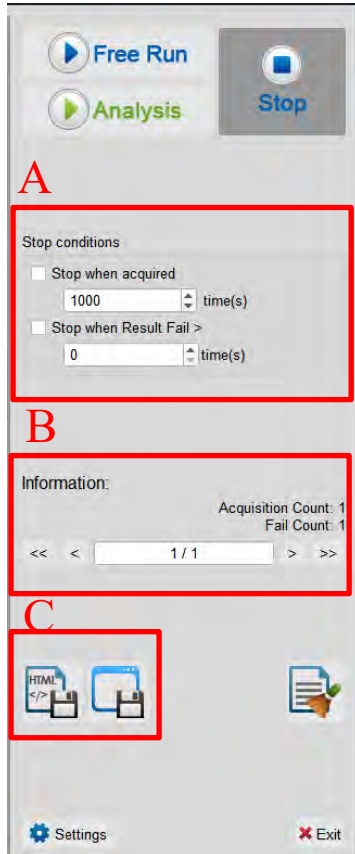
The screenshot shows the software electrical validation interface with a waveform and a data table.

**Waveform:** Shows a signal with a 200 ns scale bar. The signal is labeled 'MIPI RFFE Validation' and 'Stop Sfr: 500 MS/s'. The waveform shows a series of pulses with a period of approximately 1.5 μs.

**Data Table:**

| Timestamp | SLMID             | Command          | Byte Count | Address | Mask | Data           | Information |
|-----------|-------------------|------------------|------------|---------|------|----------------|-------------|
| 1.528 μs  | Spare (user-d...) | Register Writ... |            | 1C      |      | PM_TRIG[7:0... |             |
| 1.814 μs  |                   |                  |            |         |      | PWR_MODE       |             |
| 1.814 μs  |                   |                  |            |         |      | TRIG_REG[5     |             |
| 2.164 μs  | PA Module 1(F)    | Register Writ... |            | 1C      |      | PM_TRIG[7:0    |             |
| 2.448 μs  |                   |                  |            |         |      | PWR_MODE       |             |
| 2.448 μs  |                   |                  |            |         |      | TRIG_REG[5     |             |

## 5. Software electrical validation control panel:



### A. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

### B. Information:

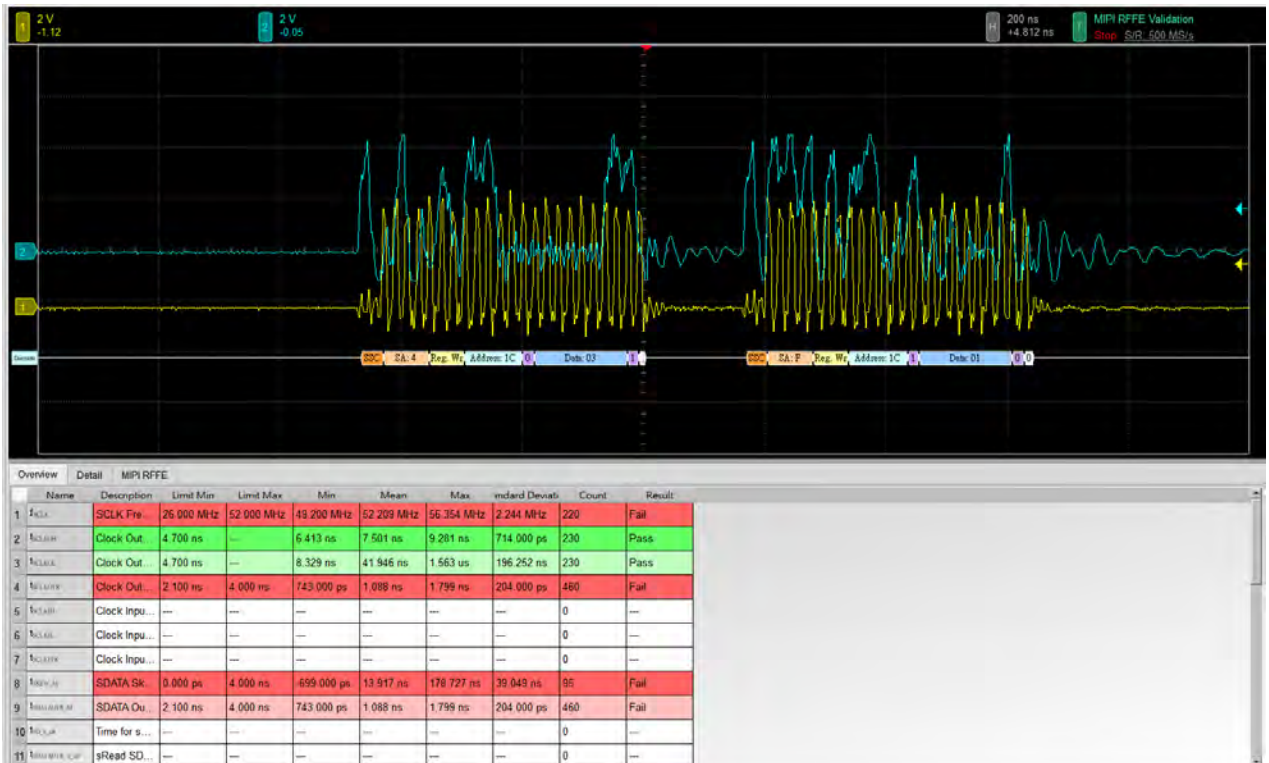
Select waveform

### C. Save File:

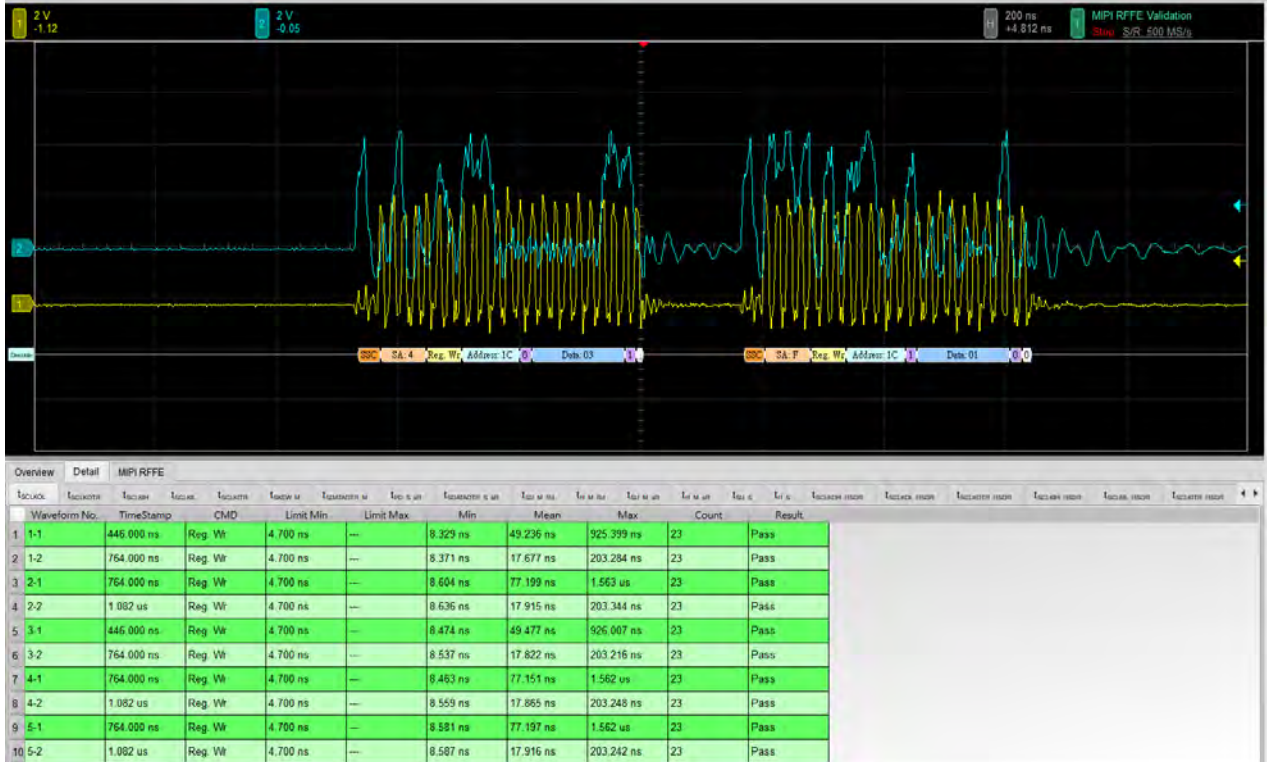
Save as Html

Save as .MOW(Software format)

## 6. Overview Report:



## 7. Detail Report:



## 8. Reference Point Dialog & Waveform:



## 9. Html Report:



### Electrical Validation Report

|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | M503124V            |
| Test Instruments Serial Number | MSV31240021         |
| Test Date                      | 12-09-2024 15:32:11 |
| S/W Version                    | 1.8.62              |
| Protocol                       | MIPI RFFE           |

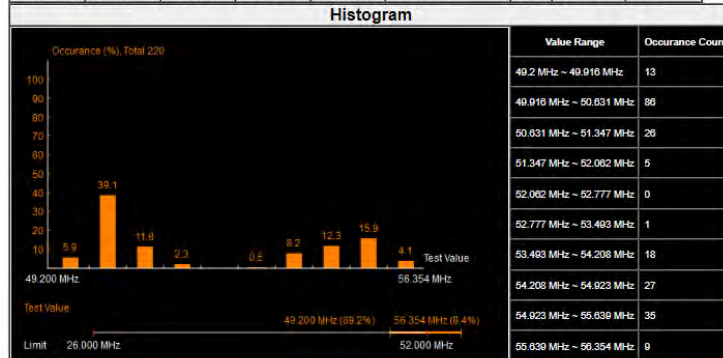
#### Overview Results:

Total: 33  
Pass: 2  
Fail: 6

| Index | Name                | Description   | Limit Min  | Limit Max  | Min         | Mean       | Max        | Standard Deviation | Count | Margin Min | Margin Max | Result |
|-------|---------------------|---|------------|------------|-------------|------------|------------|--------------------|-------|------------|------------|--------|
| 1     | fSCLK               | SCLK Frequency  | 26.000 MHz | 52.000 MHz | 49.200 MHz  | 52.209 MHz | 56.354 MHz | 2.244 MHz          | 220   | 89.2%      | 8.4%       | Fail   |
| 2     | fSCLKOH             | Clock Output High Time  | 4.700 ns   | ---        | 6.413 ns    | 7.501 ns   | 9.281 ns   | 714.000 ps         | 230   | 36.4%      | ---        | Pass   |
| 3     | fSCLKOL             | Clock Output Low Time   | 4.700 ns   | ---        | 8.329 ns    | 41.946 ns  | 1.563 ns   | 196.252 ns         | 230   | 77.2%      | ---        | Pass   |
| 4     | fSCLKOTR            | Clock Output Transition (Rise/Fall) Time                              | 2.100 ns   | 4.000 ns   | 743.000 ps  | 1.088 ns   | 1.799 ns   | 204.000 ps         | 460   | -64.6%     | -55.0%     | Fail   |
| 5     | fSCLKIH             | Clock Input High Time   | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 6     | fSCLKIL             | Clock Input Low Time  | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 7     | fSCLKITR            | Clock Input Transition (Rise/Fall) Time                               | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 8     | fSKEW_M             | SDATA Slew Relative to SCLK_BOM Master Output                         | 0.000 ps   | 4.000 ns   | -699.000 ps | 13.917 ns  | 178.727 ns | 39.049 ns          | 95    | ---        | 4368.2%    | Fail   |
| 9     | fSDATAQTR_M         | SDATA Output Transition (Rise/Fall) Time - BOM Master                 | 2.100 ns   | 4.000 ns   | 743.000 ps  | 1.088 ns   | 1.799 ns   | 204.000 ps         | 460   | -64.6%     | -55.0%     | Fail   |
| 10    | fD0_S_R             | Time for sRead Data Output Valid from SCLK Rising Edge - Slave        | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 11    | fSDATAQTR_S_R       | sRead SDATA Output Transition (Rise/Fall) Time - Slave                | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 12    | fSU_M_Rd            | SDATA Setup Time, with respect to SCLK Output - BOM - Read            | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 13    | tH_M_Rd             | SDATA Hold Time, with respect to SCLK Output - BOM - Read             | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 14    | fSU_M_sR            | SDATA Setup Time, with respect to SCLK Output - BOM - sRead           | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 15    | tH_M_sR             | SDATA Hold Time, with respect to SCLK Output - BOM - sRead            | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 16    | fSU_S               | SDATA Setup Time, with respect to SCLK Input - Slave (or non-BOM)     | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 17    | tH_S                | SDATA Hold Time, with respect to SCLK Input - Slave (or non-BOM)      | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 18    | fSCLKOH_HSDR        | (HSDR) Clock Output High Time   | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 19    | fSCLKOL_HSDR        | (HSDR) Clock Output Low Time  | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 20    | fSCLKOTR_HSDR       | (HSDR) Clock Output Transition (Rise/Fall) Time                       | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 21    | fSCLKIH_HSDR        | (HSDR) Clock Input High Time  | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 22    | fSCLKIL_HSDR        | (HSDR) Clock Input Low Time   | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 23    | fSCLKITR_HSDR       | (HSDR) Clock Input Transition (Rise/Fall) Time                        | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 24    | fD0_S_Rd_HSDR       | (HSDR) Time for Read Data Output Valid from SCLK Rising Edge - Slave  | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 25    | fSDATAQTR_S_Rd_HSDR | (HSDR) Read SDATA Output Transition (Rise/Fall) Time - Slave          | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 26    | fD0_S_sR_HSDR       | (HSDR) Time for sRead Data Output Valid from SCLK Rising Edge - Slave | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 27    | fSDATAQTR_S_sR_HSDR | (HSDR) sRead SDATA Output Transition (Rise/Fall) Time - Slave         | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 28    | fSU_M_Rd_HSDR       | (HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read     | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |
| 29    | tH_M_Rd_HSDR        | (HSDR) SDATA Hold Time, with respect to SCLK Output - BOM - Read      | ---        | ---        | ---         | ---        | ---        | ---                | 0     | ---        | ---        | ---    |

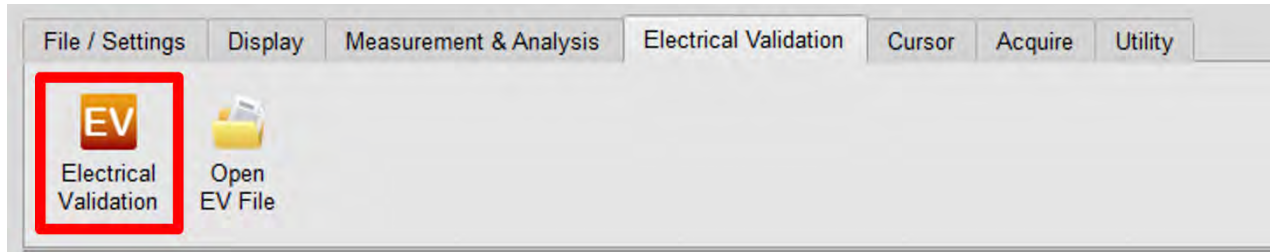
fSCLK - Test Result: **Fail**  
Description: SCLK Frequency

| Limit Min  | Limit Max  | Min        | Mean       | Max        | Standard Deviation | Count | Margin Min | Margin Max |
|------------|------------|------------|------------|------------|--------------------|-------|------------|------------|
| 26.000 MHz | 52.000 MHz | 49.200 MHz | 52.209 MHz | 56.354 MHz | 2.244 MHz          | 220   | 89.2%      | 8.4%       |



# MIPI SPMI Electrical Validation Solution

## ■ Introduction:

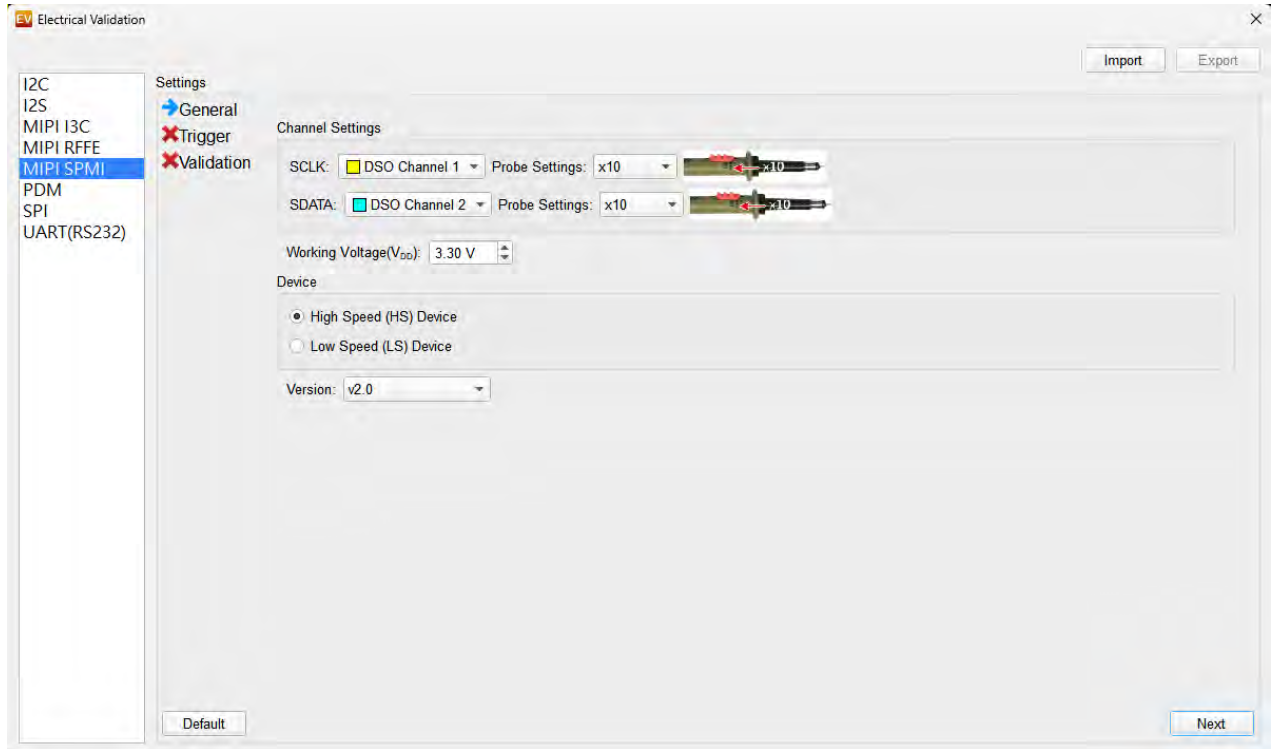


Use an oscilloscope to do MIPI SPMI Electrical Validation to ensure that the MIPI SPMI meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation.

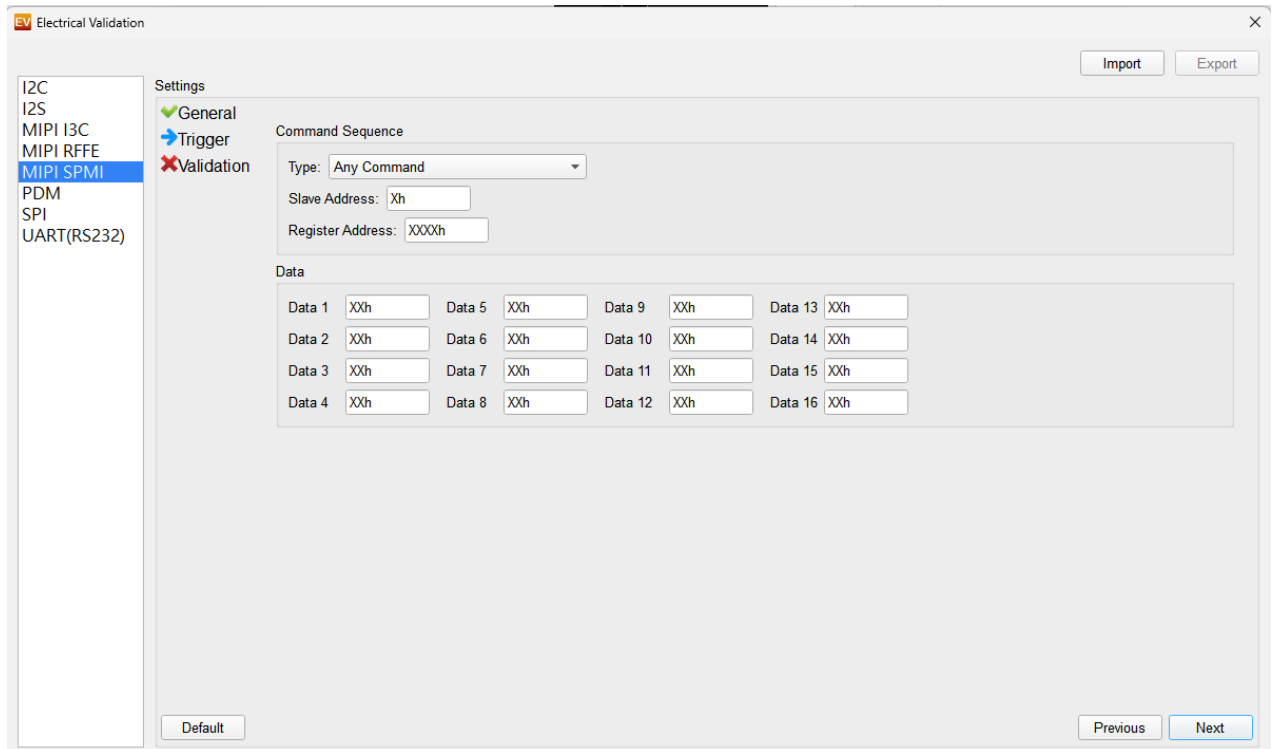
MIPI SPMI (System Power Management Interface) is a specification developed by the **MIPI Alliance** (Mobile Industry Processor Interface) for managing power in mobile and embedded systems. The primary goal of SPMI is to provide a standardized communication interface between power management ICs (PMICs) and various system components, allowing efficient power distribution and power state management in devices like smartphones, tablets, and other embedded systems.

# MIPI SPMI Electrical Validation Solution

## 1. General Setting: Channel sources, working voltage, speed and version



## 2. Trigger Setting:



### 3. Electrical validation settings: Frequency, Time and Voltage limitation

The screenshot shows the 'Electrical Validation' window with the following settings:

- Settings:** General (checked), Trigger (checked), Validation (selected).
- Customized EV Parameter:**
  - Frequency:**

| Name   | Description    | Min    | Max    |
|--|----------------|--------|--------|
| <input checked="" type="checkbox"/> f <sub>SCL</sub> | SCLK Frequency | 32 KHz | 26 MHz |
  - Time:**

| Name  | Description                              | Min    | Max    |
|---|--|--------|--------|
| <input checked="" type="checkbox"/> t <sub>SCLHIGH</sub>  | SCLK Output High Time                    | 12 ns  | X      |
| <input checked="" type="checkbox"/> t <sub>SCLLOW</sub>   | SCLK Output Low Time                     | 12 ns  | X      |
| <input checked="" type="checkbox"/> t <sub>SCLWTR</sub>   | SCLK Output Transition (Rise/Fall) Time  | 2.1 ns | 5.3 ns |
| <input checked="" type="checkbox"/> t <sub>SDATAWTR</sub> | SDATA Output Transition (Rise/Fall) Time | 2.1 ns | 5.3 ns |
| <input checked="" type="checkbox"/> t <sub>D</sub>        | SDATA Output Valid Time                  | 0 us   | 11 ns  |
| <input checked="" type="checkbox"/> t <sub>S</sub>        | SDATA Setup Time                         | 1 ns   | X      |
| <input checked="" type="checkbox"/> t <sub>H</sub>        | SDATA Hold Time                          | 5 ns   | X      |
  - Voltage:**

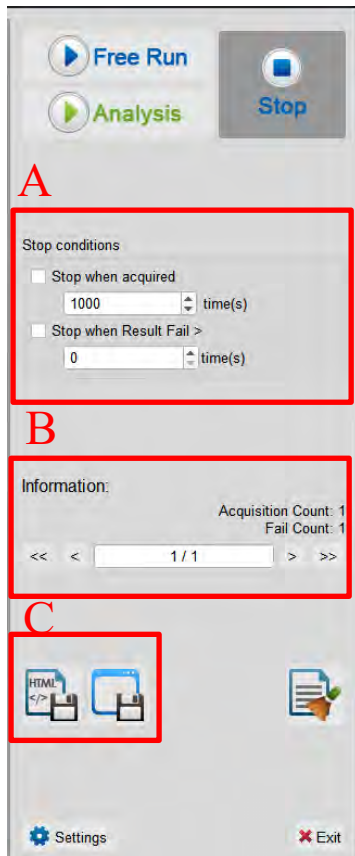
| Name   | Description        | Min    | Max    |
|--|--------------------|--------|--------|
| <input checked="" type="checkbox"/> V <sub>L</sub> | Low-Level Voltage  | 0 V    | 360 mV |
| <input checked="" type="checkbox"/> V <sub>H</sub> | High-Level Voltage | 1.44 V | 1.8 V  |

### 4. Software electrical validation interface:

The screenshot shows the software electrical validation interface with a waveform and a data table. The waveform displays a signal with a period of 1 μs and a stop time of 3.946 μs. The data table below the waveform shows the following details:

| Timestamp | Arbitration | Command                      | Addr. (h) | Req. Addr. (h) | Byte Count | Data (h) | Error |
|-----------|-------------|------------------------------|-----------|----------------|------------|----------|-------|
| 12.824 μs | MPL0        | Extended Register Write Long | SA(4)     | A140           | 1(2)       | 40 03    |       |

## 5. Software electrical validation control panel:



### A. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

### B. Information:

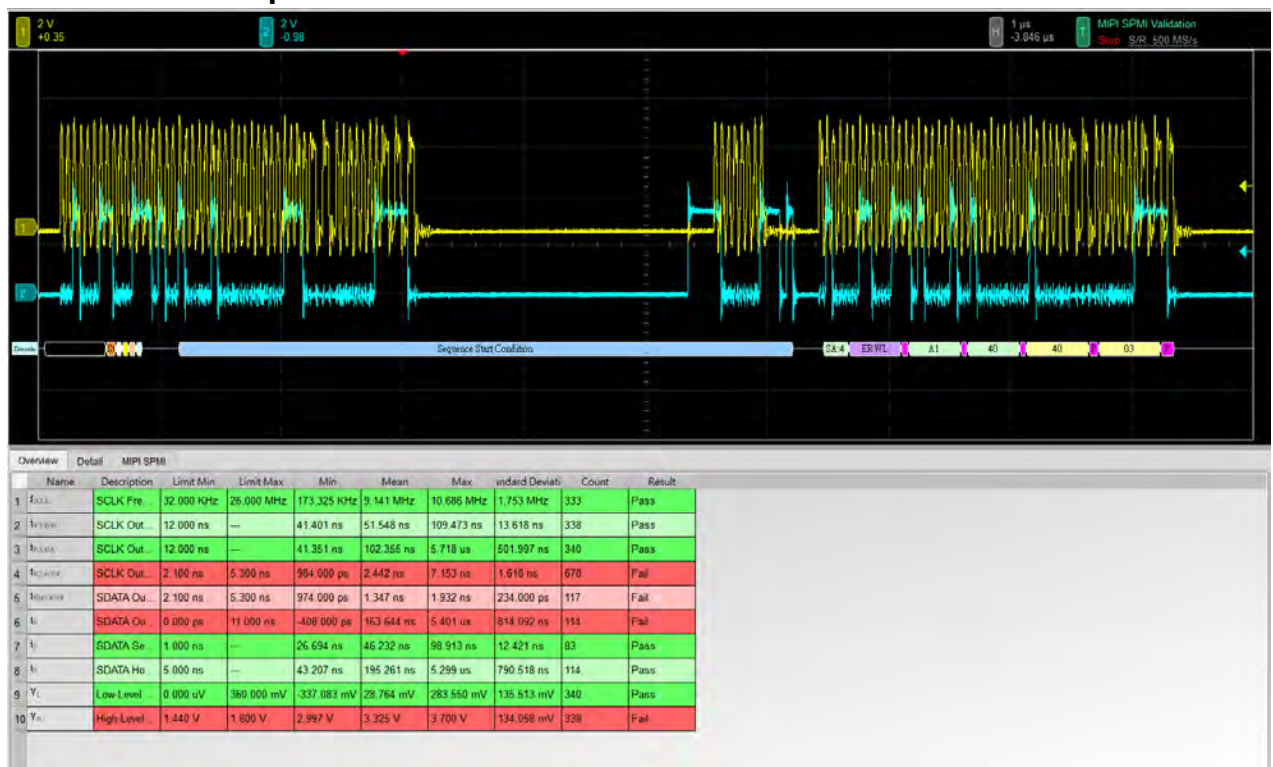
Select waveform

### C. Save File:

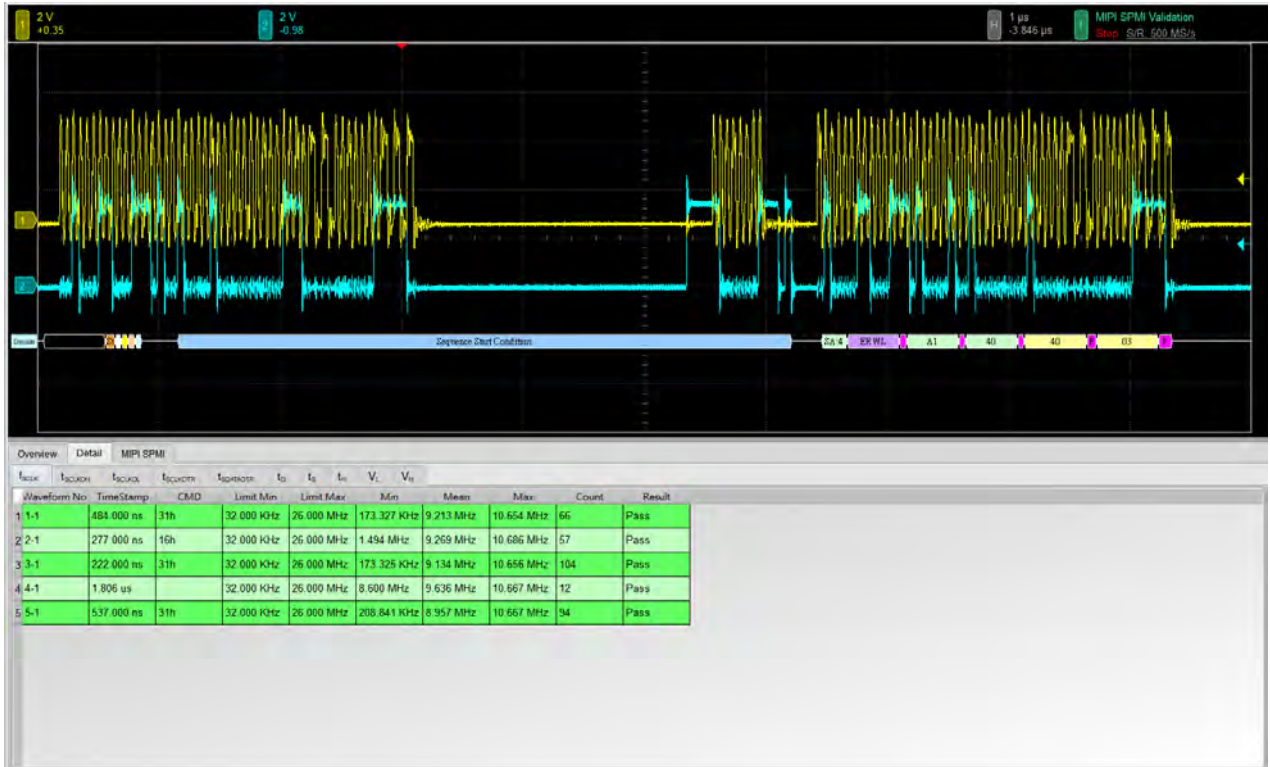
Save as Html

Save as .MOW(Software format)

## 6. Overview Report:



## 7. Detail Report:



## 8. Reference Point Dialog & Waveform:



## 9. Html Report:



### Electrical Validation Report

|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | MSO3124V            |
| Test Instruments Serial Number | MSV31240021         |
| Test Date                      | 12-09-2024 14:54:25 |
| S/W Version                    | 1.8.62              |
| Protocol                       | MIPI SPMI           |

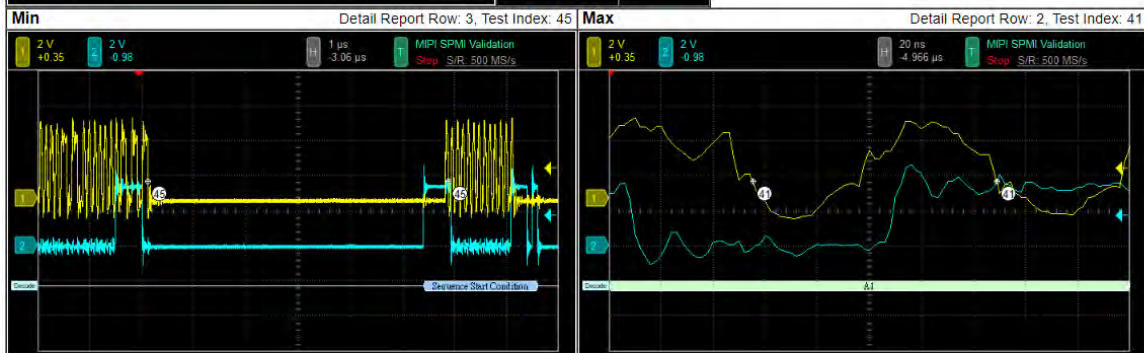
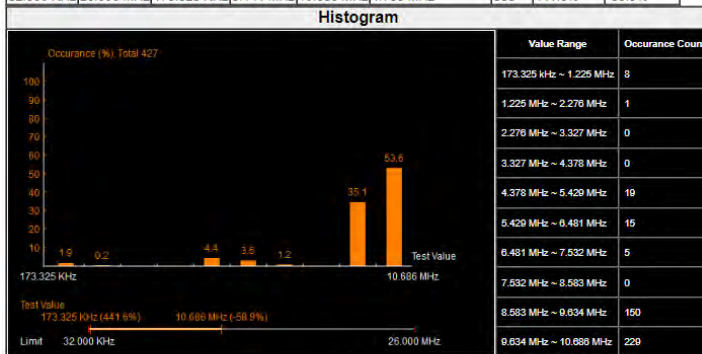
#### Overview Results:

Total: 10  
Pass: 6  
Fail: 4

| Index | Name                  | Description                              | Limit Min  | Limit Max  | Min         | Mean       | Max        | Standard Deviation | Count | Margin Min | Margin Max | Result |
|-------|-----------------------|--|------------|------------|-------------|------------|------------|--------------------|-------|------------|------------|--------|
| 1     | f <sub>SCLK</sub>     | SCLK Frequency                           | 32.000 KHz | 26.000 MHz | 173.325 KHz | 9.141 MHz  | 10.686 MHz | 1.753 MHz          | 333   | 441.6%     | -58.9%     | Pass   |
| 2     | t <sub>SCLKOH</sub>   | SCLK Output High Time                    | 12.000 ns  | ---        | 41.401 ns   | 51.548 ns  | 109.473 ns | 13.618 ns          | 338   | 245.0%     | ---        | Pass   |
| 3     | t <sub>SCLKOL</sub>   | SCLK Output Low Time                     | 12.000 ns  | ---        | 41.351 ns   | 102.355 ns | 5.718 us   | 501.997 ns         | 340   | 244.6%     | ---        | Pass   |
| 4     | t <sub>SCLKOTR</sub>  | SCLK Output Transition (Rise/Fall) Time  | 2.100 ns   | 5.300 ns   | 984.000 ps  | 2.442 ns   | 7.153 ns   | 1.618 ns           | 678   | -53.1%     | 35.0%      | Fail   |
| 5     | t <sub>SDATAOTR</sub> | SDATA Output Transition (Rise/Fall) Time | 2.100 ns   | 5.300 ns   | 974.000 ps  | 1.347 ns   | 1.932 ns   | 234.000 ps         | 117   | -53.6%     | -63.5%     | Fail   |
| 6     | t <sub>D</sub>        | SDATA Output Valid Time                  | 0.000 ps   | 11.000 ns  | -408.000 ps | 163.644 ns | 5.401 us   | 814.092 ns         | 114   | ---        | 48997.2%   | Fail   |
| 7     | t <sub>S</sub>        | SDATA Setup Time                         | 1.000 ns   | ---        | 26.694 ns   | 46.232 ns  | 98.913 ns  | 12.421 ns          | 83    | 2569.4%    | ---        | Pass   |
| 8     | t <sub>H</sub>        | SDATA Hold Time                          | 5.000 ns   | ---        | 43.207 ns   | 195.261 ns | 5.299 us   | 790.518 ns         | 114   | 764.1%     | ---        | Pass   |
| 9     | V <sub>L</sub>        | Low-Level Voltage                        | 0.000 uV   | 360.000 mV | -337.083 mV | 28.764 mV  | 283.550 mV | 135.513 mV         | 340   | ---        | -21.2%     | Pass   |
| 10    | V <sub>H</sub>        | High-Level Voltage                       | 1.440 V    | 1.800 V    | 2.997 V     | 3.325 V    | 3.700 V    | 134.058 mV         | 338   | 108.1%     | 105.5%     | Fail   |

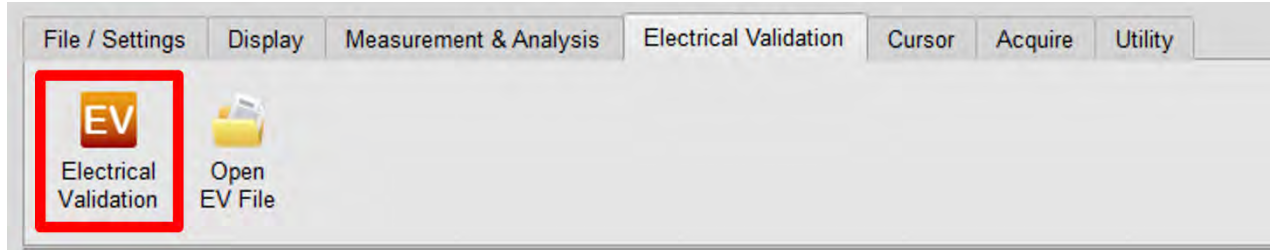
f<sub>SCLK</sub> - Test Result: **Pass**  
Description: SCLK Frequency

| Limit Min  | Limit Max  | Min         | Mean      | Max        | Standard Deviation | Count | Margin Min | Margin Max |
|------------|------------|-------------|-----------|------------|--------------------|-------|------------|------------|
| 32.000 KHz | 26.000 MHz | 173.325 KHz | 9.141 MHz | 10.686 MHz | 1.753 MHz          | 333   | 441.6%     | -58.9%     |



# PDM Electrical Validation Solution

## ■ Introduction:



Use an oscilloscope to do PCM Electrical Validation to ensure that the PDM meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

PDM Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the PDM baud rate.

Part of the electrical characteristics of common PDM specifications:

| DIGITAL AUDIO INTERFACE      |                 |  |      |      |     |
|------------------------------|-----------------|--|------|------|-----|
| PDM_CLK High Frequency Range | $f_{CLKH}$      |  | 5.28 | 8.64 | MHz |
| PDM_CLK Low Frequency Range  | $f_{CLKL}$      |  | 1.84 | 4.32 | MHz |
| PDM_CLK High Time            | $t_{PDM\_CLKH}$ |  | 40   |      | ns  |
| PDM_CLK Low Time             | $t_{PDM\_CLKL}$ |  | 40   |      | ns  |

The report of common PDM validation:

| Overview |                   |                |            |            |            |            |            |                 |       |        |
|----------|-------------------|----------------|------------|------------|------------|------------|------------|-----------------|-------|--------|
| Detail   |                   |                |            |            |            |            |            |                 |       |        |
| PDM      |                   |                |            |            |            |            |            |                 |       |        |
|          | Name              | Description    | Limit Min  | Limit Max  | Min        | Mean       | Max        | Standard Deviat | Count | Result |
| 1        | f <sub>CLK</sub>  | Clock freq...  | 0.000 Hz   | 3.072 MHz  | 3.027 MHz  | 3.030 MHz  | 3.034 MHz  | 17.798 KHz      | 4430  | Pass   |
| 2        | t <sub>LOW</sub>  | Low Perio...   | 130.208 ns | 195.312 ns | 163.008 ns | 163.289 ns | 163.541 ns | 1.399 ns        | 4920  | Pass   |
| 3        | t <sub>HIGH</sub> | High Perio...  | 130.208 ns | 195.312 ns | 163.162 ns | 163.428 ns | 163.717 ns | 1.709 ns        | 4920  | Pass   |
| 4        | t <sub>CL</sub>   | Rise time ...  | ---        | 13.000 ns  | 1.380 ns   | 1.621 ns   | 1.859 ns   | 2.428 ns        | 4930  | Pass   |
| 5        | t <sub>CL</sub>   | Fall time o... | ---        | 13.000 ns  | 1.412 ns   | 1.661 ns   | 1.862 ns   | 2.529 ns        | 4930  | Pass   |
| 6        | t <sub>DD</sub>   | Delay time...  | 40.000 ns  | 80.000 ns  | 57.382 ns  | 64.017 ns  | 74.913 ns  | 77.763 ns       | 2500  | Pass   |
| 7        | t <sub>DV</sub>   | Delay time...  | ---        | 100.000 ns | 60.111 ns  | 67.555 ns  | 79.252 ns  | 83.904 ns       | 2500  | Pass   |
| 8        | t <sub>DD</sub>   | Delay time...  | 40.000 ns  | 80.000 ns  | 54.659 ns  | 60.684 ns  | 71.123 ns  | 67.169 ns       | 2440  | Pass   |
| 9        | t <sub>DV</sub>   | Delay time...  | ---        | 100.000 ns | 57.573 ns  | 64.149 ns  | 75.158 ns  | 71.543 ns       | 2440  | Pass   |

Dedicated page for Electrical Validation:



5. Frequency: Clock speed
6. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
7. Voltage: VL, VH, etc.

Frequency:

| Symbol    | Electrical Parameter    |
|-----------|-------------------------|
| $f_{SCL}$ | PDM_CLK Frequency Range |

Time:

| Symbol     | Electrical Parameter                           |
|------------|--|
| $t_{LOW}$  | Low Period of the Clock                        |
| $t_{HIGH}$ | High Period of the Clock                       |
| $t_{rCL}$  | Rise time of Clock signal                      |
| $t_{fCL}$  | Fall time of Clock signal                      |
| $t_{rDD}$  | Delay time from Clock edge to Data Rise driven |
| $t_{fDD}$  | Delay time from Clock edge to Data Fall driven |
| $t_{rDV}$  | Delay time from Clock edge to Data Rise valid  |
| $t_{fDV}$  | Delay time from Clock edge to Data Fall valid  |

Voltage:

| Symbol         | Electrical Parameter               |
|----------------|------------------------------------|
| $V_{ClkLow}$   | Low-level Input voltage for clock  |
| $V_{ClkHigh}$  | High-level Input voltage for clock |
| $V_{DataLow}$  | Low-level Input voltage for data   |
| $V_{DataHigh}$ | High-level Input voltage for data  |


## ■ PDM Electrical Validation Settings:


### 1. General Settings: Channel sources, working voltage and speed

Settings

- ➔ General
- ✖ Decode
- ✖ Validation

Channel Settings

CLK:  Probe Settings:  

DATA:  Probe Settings:  

Working Voltage(V<sub>DD</sub>):

PDM Clock Speed:  KHz

## 2. Decode Settings: PDM decoding settings

Settings

- ✔ General
- ➔ Decode
- ✘ Validation

Audio Settings

Decimation Rate: x64

Audio Frequency: 48 KHz

Mono & Stereo

Mode: Stereo

Default Previous Next

### 3. Electrical validation settings: Voltage, timing, frequency limitation

Settings

- General
- Decode
- Validation

Customized EV Parameter:

**Frequency**

| Name  | Description     | Min   | Max       |
|---|-----------------|-------|-----------|
| 1 <input checked="" type="checkbox"/> $f_{CLK}$ | Clock frequency | 0 kHz | 3.072 MHz |

**Time**

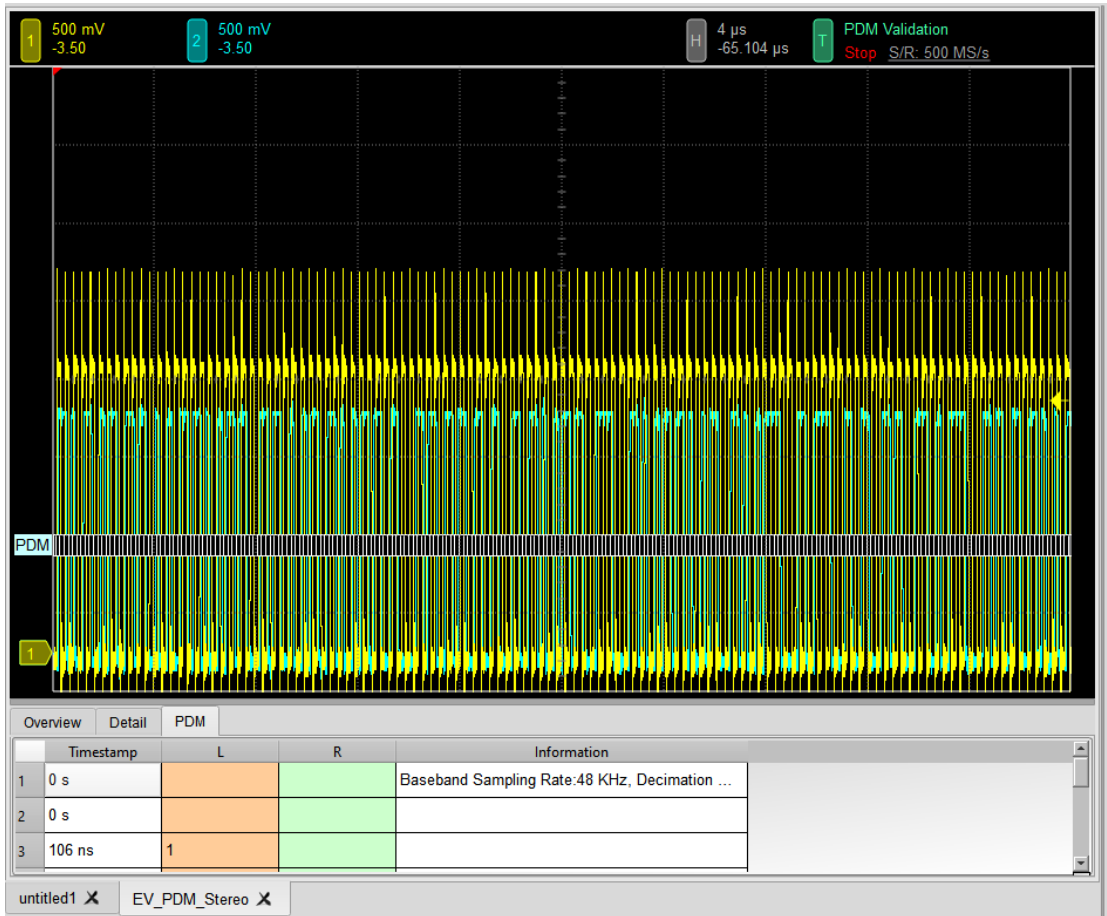
| Name   | Description                                  | Min        | Max        |
|--|--|------------|------------|
| 1 <input checked="" type="checkbox"/> $t_{LOW}$  | Low Period of the Clock                      | 130.208 ns | 195.312 ns |
| 2 <input checked="" type="checkbox"/> $t_{HIGH}$ | High Period of the Clock                     | 130.208 ns | 195.312 ns |
| 3 <input checked="" type="checkbox"/> $t_{RC}$   | Rise time of CLK signal                      | X          | 13 ns      |
| 4 <input checked="" type="checkbox"/> $t_{FC}$   | Fall time of CLK signal                      | X          | 13 ns      |
| 5 <input checked="" type="checkbox"/> $t_{RDO}$  | Delay time from Clk edge to Data Rise driven | 40 ns      | 80 ns      |
| 6 <input checked="" type="checkbox"/> $t_{FDO}$  | Delay time from Clk edge to Data Fall driven | 40 ns      | 80 ns      |
| 7 <input checked="" type="checkbox"/> $t_{RDV}$  | Delay time from Clk edge to Data Rise Valid  | X          | 100 ns     |
| 8 <input checked="" type="checkbox"/> $t_{FDV}$  | Delay time from Clk edge to Data Fall Valid  | X          | 100 ns     |

**Voltage**

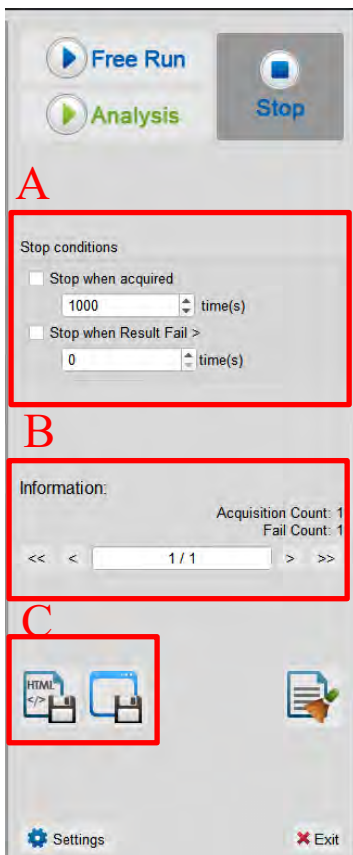
| Name  | Description                        | Min    | Max    |
|---|------------------------------------|--------|--------|
| 1 <input checked="" type="checkbox"/> $V_{CLK,low}$   | Low-level input voltage for clock  | -0.5 V | 0.54 V |
| 2 <input checked="" type="checkbox"/> $V_{CLK,high}$  | High-level input voltage for clock | 1.26 V | 2.3 V  |
| 3 <input checked="" type="checkbox"/> $V_{Data,low}$  | Low-level input voltage for Data   | -0.5 V | 0.54 V |
| 4 <input checked="" type="checkbox"/> $V_{Data,high}$ | High-level input voltage for Data  | 1.26 V | 2.3 V  |

Default    Advance    Previous    Apply

#### 4. Software electrical validation interface:



#### 5. Software electrical validation control panel:



##### A. Stop Conditions:

- Stop when acquired X times
- Stop when Result Fail > X times

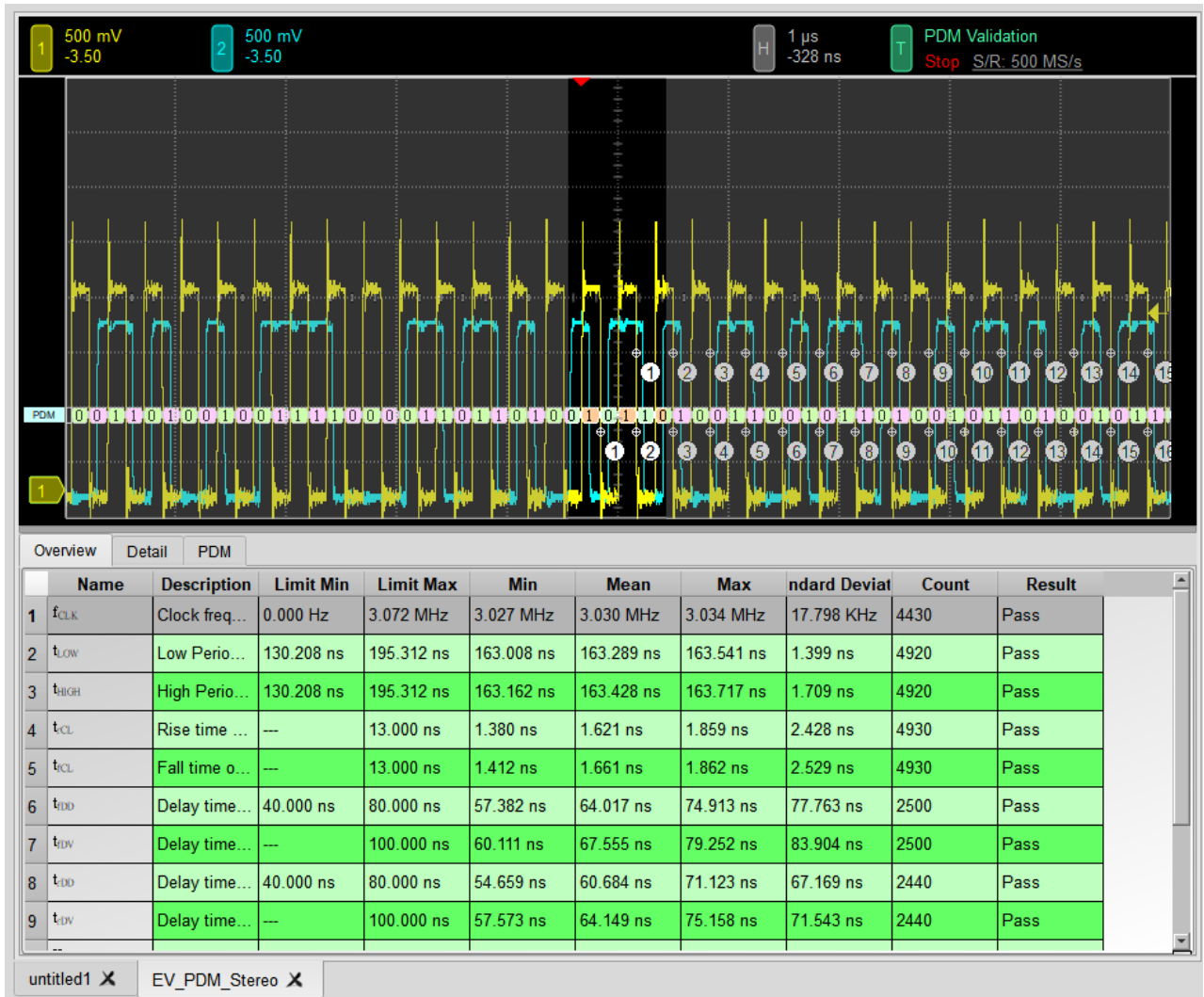
##### B. Information:

- Select waveform

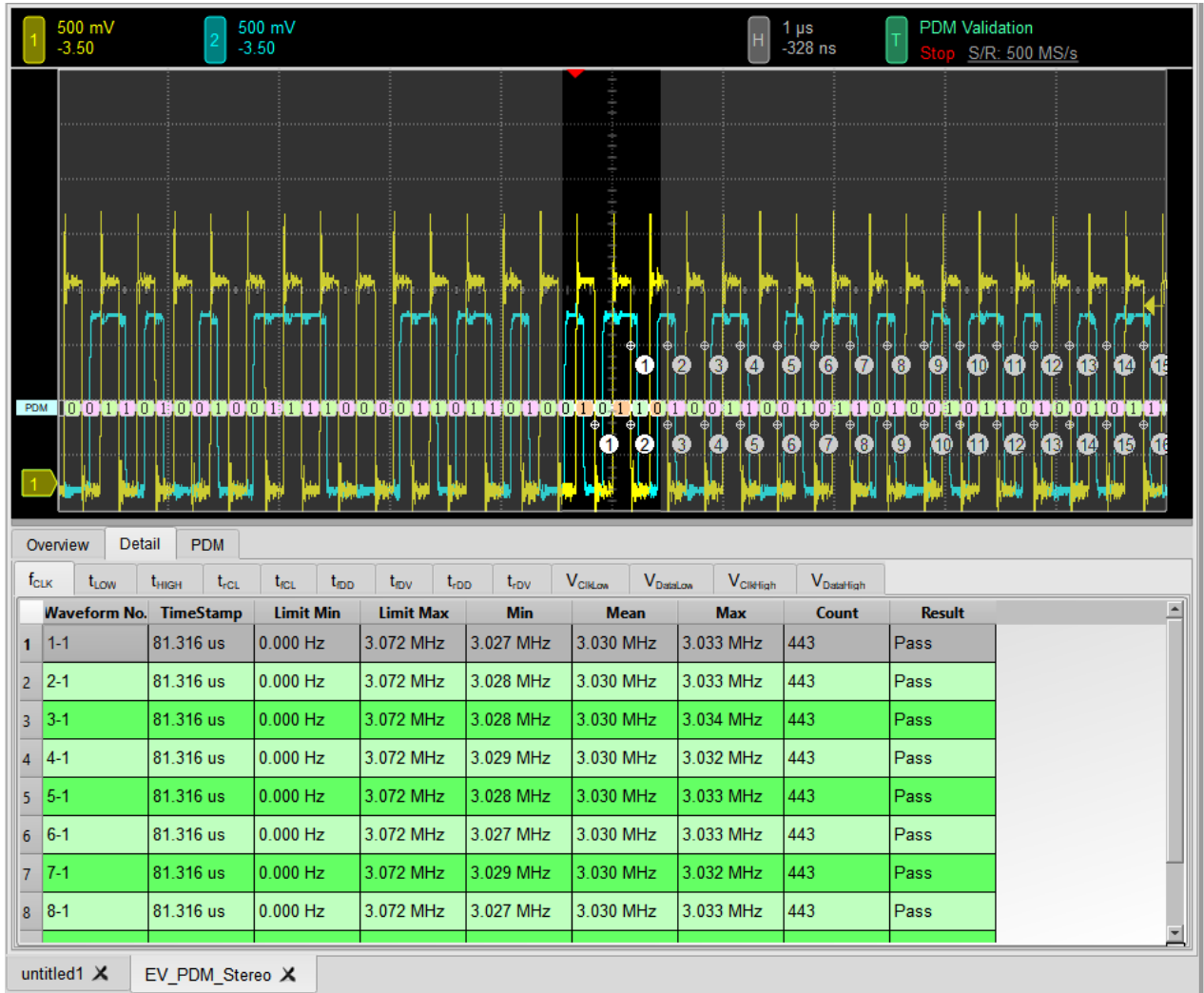
##### C. Save File:

- Save as Html
- Save as .MOW(Software format)

## 6. Overview Report:



## 7. Detail Report:



## 8. Reference Point Dialog & Waveform:



## 9. Html Report:



### Electrical Validation Report

|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | MSO3124V            |
| Test Instruments Serial Number | MSV31240017         |
| Test Date                      | 09-21-2023 10:27:35 |
| S/W Version                    | 1.7.59              |
| Protocol                       | PDM                 |

PDM Testing

#### Overview Results:

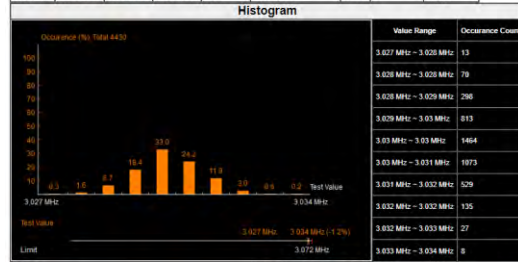
Total: 13  
Pass: 13  
Fail: 0

| Index | Name                  | Description                                  | Limit Min   | Limit Max  | Min        | Mean       | Max        | Standard Deviation | Count | Margin Min | Margin Max | Result |
|-------|-----------------------|--|-------------|------------|------------|------------|------------|--------------------|-------|------------|------------|--------|
| 1     | f <sub>CLK</sub>      | Clock frequency                              | 0.000 Hz    | 3.072 MHz  | 3.027 MHz  | 3.030 MHz  | 3.034 MHz  | 17.798 KHz         | 4430  | ---        | -1.2%      | Pass   |
| 2     | t <sub>LOW</sub>      | Low Period of the Clock                      | 130.208 ns  | 195.312 ns | 163.008 ns | 163.289 ns | 163.541 ns | 1.399 ns           | 4920  | 25.2%      | -16.3%     | Pass   |
| 3     | t <sub>HIGH</sub>     | High Period of the Clock                     | 130.208 ns  | 195.312 ns | 163.162 ns | 163.428 ns | 163.717 ns | 1.709 ns           | 4920  | 25.3%      | -16.2%     | Pass   |
| 4     | t <sub>CL</sub>       | Rise time of CLK signal                      | ---         | 13.000 ns  | 1.380 ns   | 1.621 ns   | 1.859 ns   | 2.428 ns           | 4930  | ---        | -85.7%     | Pass   |
| 5     | t <sub>CL</sub>       | Fall time of CLK signal                      | ---         | 13.000 ns  | 1.412 ns   | 1.661 ns   | 1.962 ns   | 2.529 ns           | 4930  | ---        | -85.7%     | Pass   |
| 6     | t <sub>DD</sub>       | Delay time from Clk edge to Data Fail driven | 40.000 ns   | 80.000 ns  | 57.382 ns  | 64.017 ns  | 74.913 ns  | 77.763 ns          | 2500  | 43.5%      | -6.4%      | Pass   |
| 7     | t <sub>DV</sub>       | Delay time from Clk edge to Data Fail Valid  | ---         | 100.000 ns | 60.111 ns  | 67.555 ns  | 79.252 ns  | 83.904 ns          | 2500  | ---        | -20.7%     | Pass   |
| 8     | t <sub>DD</sub>       | Delay time from Clk edge to Data Rise driven | 40.000 ns   | 80.000 ns  | 54.659 ns  | 60.684 ns  | 71.123 ns  | 67.169 ns          | 2440  | 36.6%      | -11.1%     | Pass   |
| 9     | t <sub>DV</sub>       | Delay time from Clk edge to Data Rise Valid  | ---         | 100.000 ns | 57.573 ns  | 64.149 ns  | 75.156 ns  | 71.543 ns          | 2440  | ---        | -24.8%     | Pass   |
| 10    | V <sub>CLLow</sub>    | Low-level input voltage for clock            | -500.000 mV | 540.000 mV | -56.786 mV | -50.438 mV | -42.405 mV | 49.004 mV          | 4920  | -88.8%     | -107.8%    | Pass   |
| 11    | V <sub>DataLow</sub>  | Low-level input voltage for Data             | -500.000 mV | 540.000 mV | -55.069 mV | -49.177 mV | -35.569 mV | 51.321 mV          | 2467  | -89.0%     | -106.6%    | Pass   |
| 12    | V <sub>CLHigh</sub>   | High-level input voltage for clock           | 1.260 V     | 2.300 V    | 1.825 V    | 1.835 V    | 1.850 V    | 93.739 mV          | 4930  | 44.8%      | -19.6%     | Pass   |
| 13    | V <sub>DataHigh</sub> | High-level input voltage for Data            | 1.260 V     | 2.300 V    | 1.499 V    | 1.515 V    | 1.531 V    | 77.266 mV          | 2467  | 19.0%      | -33.4%     | Pass   |

#### f<sub>CLK</sub> - Test Result: Pass

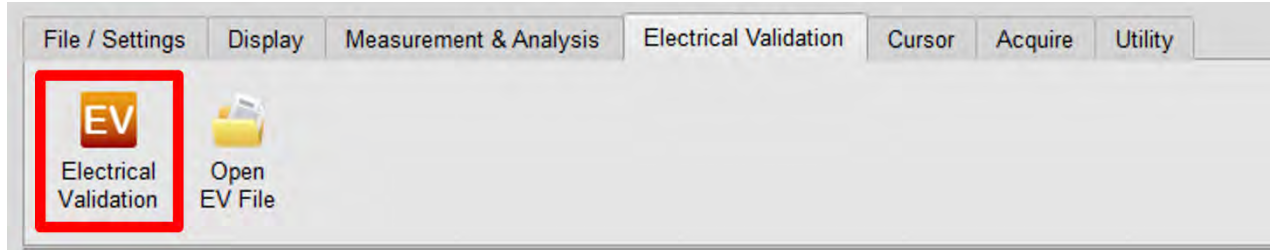
Description: Clock frequency

| Limit Min | Limit Max | Min       | Mean      | Max       | Standard Deviation | Count | Margin Min | Margin Max |
|-----------|-----------|-----------|-----------|-----------|--------------------|-------|------------|------------|
| 0.000 Hz  | 3.072 MHz | 3.027 MHz | 3.030 MHz | 3.034 MHz | 17.798 KHz         | 4430  | ---        | -1.2%      |



# SMBUS Electrical Validation Solution

## ■ Introduction:



Use an oscilloscope to do PCM Electrical Validation to ensure that the PDM meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

PDM Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the PDM baud rate.

Part of the electrical characteristics of common PDM specifications:

| DIGITAL AUDIO INTERFACE      |                 |  |      |      |     |
|------------------------------|-----------------|--|------|------|-----|
| PDM_CLK High Frequency Range | $f_{CLKH}$      |  | 5.28 | 8.64 | MHz |
| PDM_CLK Low Frequency Range  | $f_{CLKL}$      |  | 1.84 | 4.32 | MHz |
| PDM_CLK High Time            | $t_{PDM\_CLKH}$ |  | 40   |      | ns  |
| PDM_CLK Low Time             | $t_{PDM\_CLKL}$ |  | 40   |      | ns  |

The report of common PDM validation:

|   | Name              | Description    | Limit Min  | Limit Max  | Min        | Mean       | Max        | Standard Deviat | Count | Result |
|---|-------------------|----------------|------------|------------|------------|------------|------------|-----------------|-------|--------|
| 1 | f <sub>CLK</sub>  | Clock freq...  | 0.000 Hz   | 3.072 MHz  | 3.027 MHz  | 3.030 MHz  | 3.034 MHz  | 17.798 KHz      | 4430  | Pass   |
| 2 | t <sub>LOW</sub>  | Low Perio...   | 130.208 ns | 195.312 ns | 163.008 ns | 163.289 ns | 163.541 ns | 1.399 ns        | 4920  | Pass   |
| 3 | t <sub>HIGH</sub> | High Perio...  | 130.208 ns | 195.312 ns | 163.162 ns | 163.428 ns | 163.717 ns | 1.709 ns        | 4920  | Pass   |
| 4 | t <sub>CL</sub>   | Rise time ...  | ---        | 13.000 ns  | 1.380 ns   | 1.621 ns   | 1.859 ns   | 2.428 ns        | 4930  | Pass   |
| 5 | t <sub>CL</sub>   | Fall time o... | ---        | 13.000 ns  | 1.412 ns   | 1.661 ns   | 1.862 ns   | 2.529 ns        | 4930  | Pass   |
| 6 | t <sub>DD</sub>   | Delay time...  | 40.000 ns  | 80.000 ns  | 57.382 ns  | 64.017 ns  | 74.913 ns  | 77.763 ns       | 2500  | Pass   |
| 7 | t <sub>DV</sub>   | Delay time...  | ---        | 100.000 ns | 60.111 ns  | 67.555 ns  | 79.252 ns  | 83.904 ns       | 2500  | Pass   |
| 8 | t <sub>DD</sub>   | Delay time...  | 40.000 ns  | 80.000 ns  | 54.659 ns  | 60.684 ns  | 71.123 ns  | 67.169 ns       | 2440  | Pass   |
| 9 | t <sub>DV</sub>   | Delay time...  | ---        | 100.000 ns | 57.573 ns  | 64.149 ns  | 75.158 ns  | 71.543 ns       | 2440  | Pass   |

Dedicated page for Electrical Validation:



8. Frequency: Clock speed

9. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation

10. Voltage: VL, VH, etc.

Frequency:

| Symbol    | Electrical Parameter    |
|-----------|-------------------------|
| $f_{SCL}$ | PDM_CLK Frequency Range |

Time:

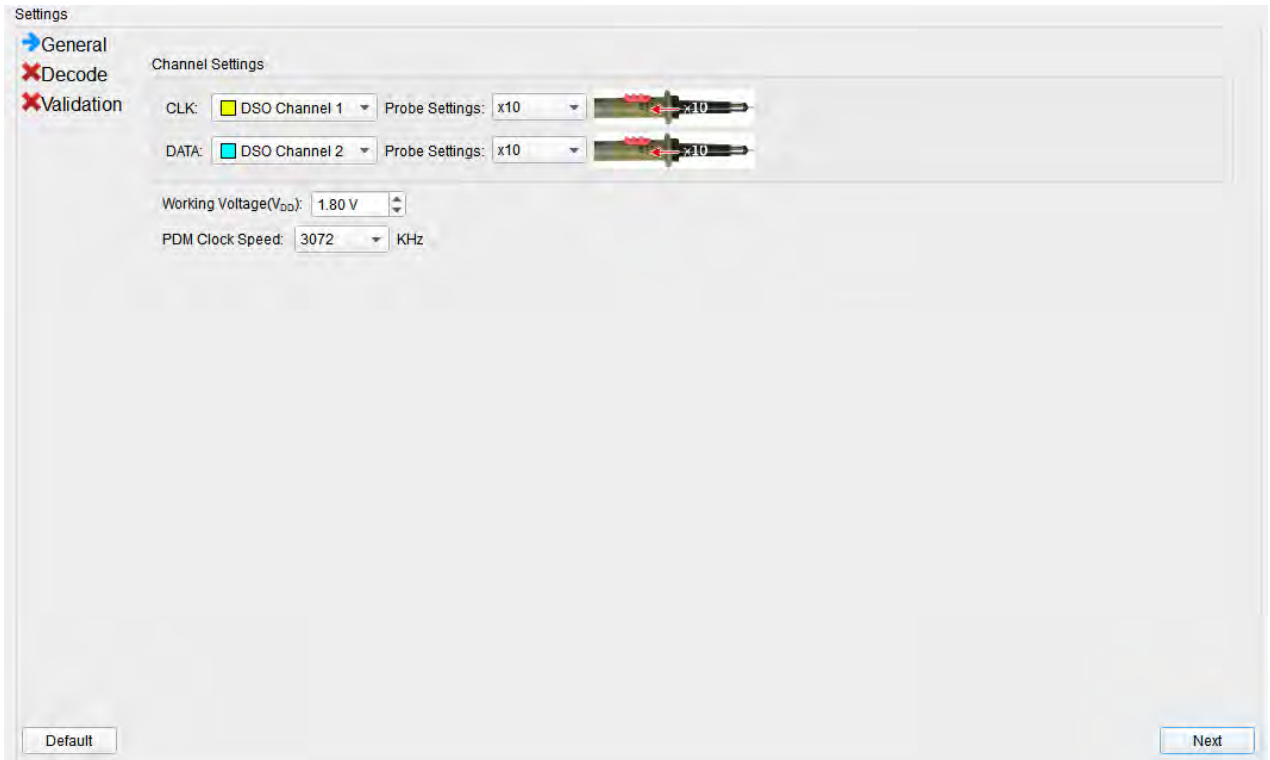
| Symbol     | Electrical Parameter                           |
|------------|--|
| $t_{LOW}$  | Low Period of the Clock                        |
| $t_{HIGH}$ | High Period of the Clock                       |
| $t_{rCL}$  | Rise time of Clock signal                      |
| $t_{fCL}$  | Fall time of Clock signal                      |
| $t_{rDD}$  | Delay time from Clock edge to Data Rise driven |
| $t_{fDD}$  | Delay time from Clock edge to Data Fall driven |
| $t_{rDV}$  | Delay time from Clock edge to Data Rise valid  |
| $t_{fDV}$  | Delay time from Clock edge to Data Fall valid  |

Voltage:

| Symbol         | Electrical Parameter               |
|----------------|------------------------------------|
| $V_{ClkLow}$   | Low-level Input voltage for clock  |
| $V_{ClkHigh}$  | High-level Input voltage for clock |
| $V_{DataLow}$  | Low-level Input voltage for data   |
| $V_{DataHigh}$ | High-level Input voltage for data  |

## ■ SMBUS Electrical Validation Settings:

### 1. General Settings: Channel sources, working voltage and speed



## 2. Decode Settings: PDM decoding settings

Settings

- ✔ General
- ➔ Decode
- ✘ Validation

Audio Settings

Decimation Rate: x64

Audio Frequency: 48 KHz

Mono & Stereo

Mode: Stereo

Default Previous Next

### 3. Electrical validation settings: Voltage, timing, frequency limitation

Settings

- General
- Decode
- Validation

Customized EV Parameter:

**Frequency**

| Name  | Description     | Min   | Max       |
|---|-----------------|-------|-----------|
| 1 <input checked="" type="checkbox"/> $f_{CLK}$ | Clock frequency | 0 kHz | 3.072 MHz |

**Time**

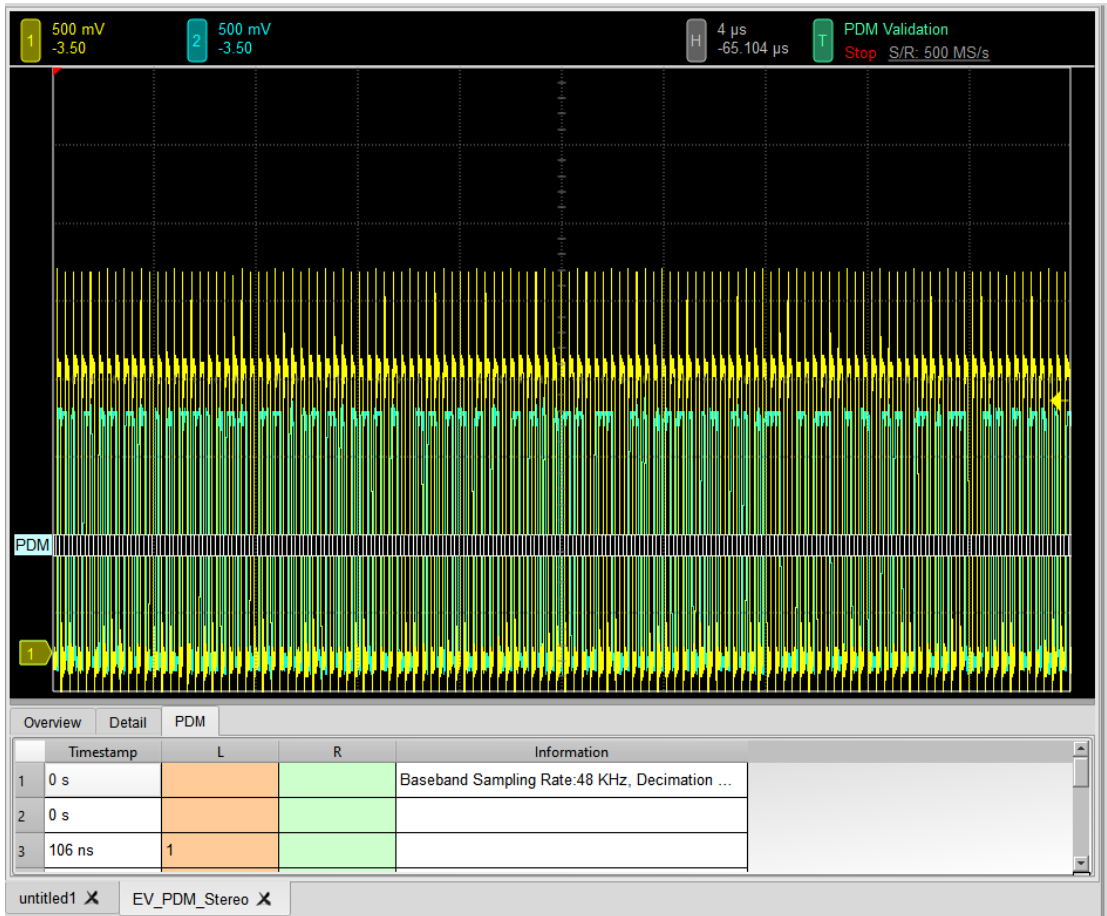
| Name   | Description                                  | Min        | Max        |
|--|--|------------|------------|
| 1 <input checked="" type="checkbox"/> $t_{LOW}$  | Low Period of the Clock                      | 130.208 ns | 195.312 ns |
| 2 <input checked="" type="checkbox"/> $t_{HIGH}$ | High Period of the Clock                     | 130.208 ns | 195.312 ns |
| 3 <input checked="" type="checkbox"/> $t_{RC}$   | Rise time of CLK signal                      | X          | 13 ns      |
| 4 <input checked="" type="checkbox"/> $t_{FC}$   | Fall time of CLK signal                      | X          | 13 ns      |
| 5 <input checked="" type="checkbox"/> $t_{RDO}$  | Delay time from Clk edge to Data Rise driven | 40 ns      | 80 ns      |
| 6 <input checked="" type="checkbox"/> $t_{FDO}$  | Delay time from Clk edge to Data Fall driven | 40 ns      | 80 ns      |
| 7 <input checked="" type="checkbox"/> $t_{RDV}$  | Delay time from Clk edge to Data Rise Valid  | X          | 100 ns     |
| 8 <input checked="" type="checkbox"/> $t_{FDV}$  | Delay time from Clk edge to Data Fall Valid  | X          | 100 ns     |

**Voltage**

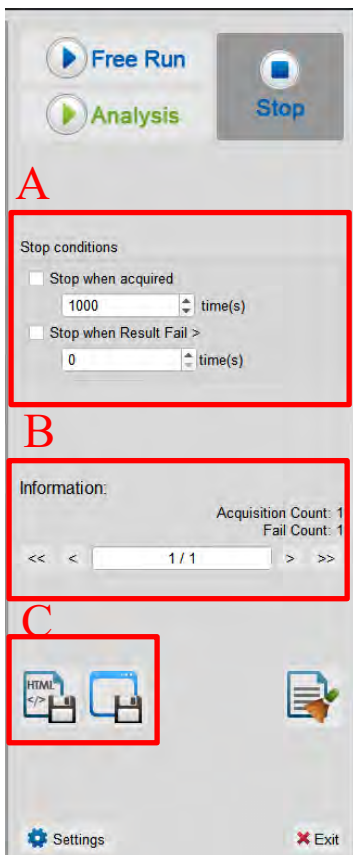
| Name  | Description                        | Min    | Max    |
|---|------------------------------------|--------|--------|
| 1 <input checked="" type="checkbox"/> $V_{CLK,low}$   | Low-level input voltage for clock  | -0.5 V | 0.54 V |
| 2 <input checked="" type="checkbox"/> $V_{CLK,high}$  | High-level input voltage for clock | 1.26 V | 2.3 V  |
| 3 <input checked="" type="checkbox"/> $V_{Data,low}$  | Low-level input voltage for Data   | -0.5 V | 0.54 V |
| 4 <input checked="" type="checkbox"/> $V_{Data,high}$ | High-level input voltage for Data  | 1.26 V | 2.3 V  |

Default    Advance    Previous    Apply

#### 4. Software electrical validation interface:



#### 5. Software electrical validation control panel:



#### D. Stop Conditions:

- Stop when acquired X times
- Stop when Result Fail > X times

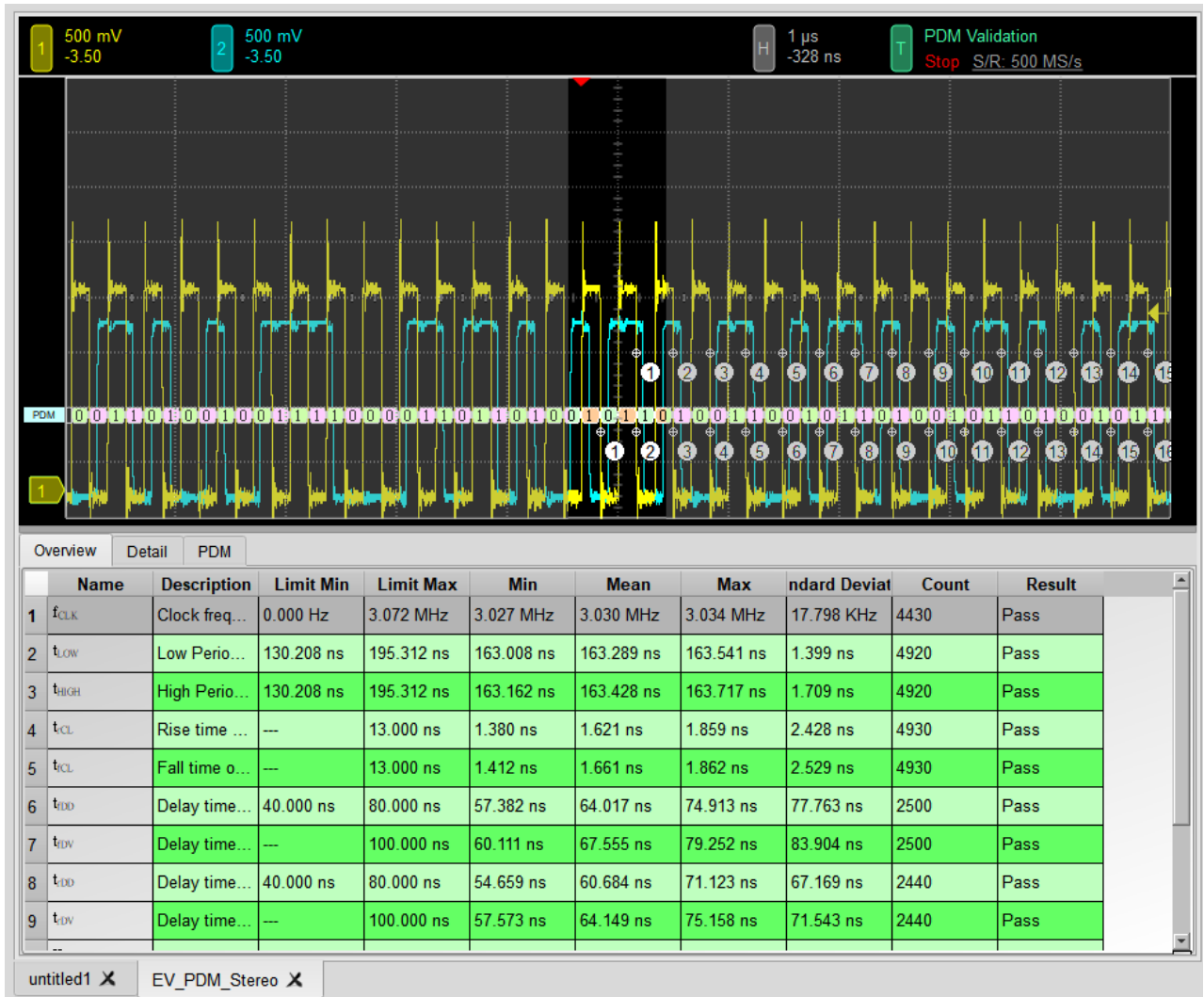
#### E. Information:

- Select waveform

#### F. Save File:

- Save as Html
- Save as .MOW(Software format)

## 6. Overview Report:





## 8. Reference Point Dialog & Waveform:



## 9. Html Report:



### Electrical Validation Report

|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | MSO3124V            |
| Test Instruments Serial Number | MSV31240017         |
| Test Date                      | 09-21-2023 10:27:35 |
| S/W Version                    | 1.7.59              |
| Protocol                       | PDM                 |

PDM Testing

#### Overview Results:

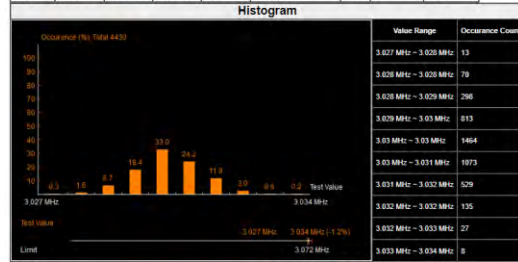
Total: 13  
Pass: 13  
Fail: 0

| Index | Name                  | Description                                  | Limit Min   | Limit Max  | Min        | Mean       | Max        | Standard Deviation | Count | Margin Min | Margin Max | Result |
|-------|-----------------------|--|-------------|------------|------------|------------|------------|--------------------|-------|------------|------------|--------|
| 1     | f <sub>CLK</sub>      | Clock frequency                              | 0.000 Hz    | 3.072 MHz  | 3.027 MHz  | 3.030 MHz  | 3.034 MHz  | 17.798 KHz         | 4430  | ---        | -1.2%      | Pass   |
| 2     | t <sub>LOW</sub>      | Low Period of the Clock                      | 130.208 ns  | 195.312 ns | 163.008 ns | 163.289 ns | 163.541 ns | 1.399 ns           | 4920  | 25.2%      | -16.3%     | Pass   |
| 3     | t <sub>HIGH</sub>     | High Period of the Clock                     | 130.208 ns  | 195.312 ns | 163.162 ns | 163.428 ns | 163.717 ns | 1.709 ns           | 4920  | 25.3%      | -16.2%     | Pass   |
| 4     | t <sub>R</sub>        | Rise time of CLK signal                      | ---         | 13.000 ns  | 1.380 ns   | 1.621 ns   | 1.859 ns   | 2.428 ns           | 4930  | ---        | -85.7%     | Pass   |
| 5     | t <sub>F</sub>        | Fall time of CLK signal                      | ---         | 13.000 ns  | 1.412 ns   | 1.661 ns   | 1.962 ns   | 2.529 ns           | 4930  | ---        | -85.7%     | Pass   |
| 6     | t <sub>DD</sub>       | Delay time from Clk edge to Data Fail driven | 40.000 ns   | 80.000 ns  | 57.382 ns  | 64.017 ns  | 74.913 ns  | 77.763 ns          | 2500  | 43.5%      | -6.4%      | Pass   |
| 7     | t <sub>DD</sub>       | Delay time from Clk edge to Data Fail Valid  | ---         | 100.000 ns | 60.111 ns  | 67.555 ns  | 79.252 ns  | 83.904 ns          | 2500  | ---        | -20.7%     | Pass   |
| 8     | t <sub>DD</sub>       | Delay time from Clk edge to Data Rise driven | 40.000 ns   | 80.000 ns  | 54.659 ns  | 60.684 ns  | 71.123 ns  | 67.169 ns          | 2440  | 36.6%      | -11.1%     | Pass   |
| 9     | t <sub>DD</sub>       | Delay time from Clk edge to Data Rise Valid  | ---         | 100.000 ns | 57.573 ns  | 64.149 ns  | 75.158 ns  | 71.543 ns          | 2440  | ---        | -24.8%     | Pass   |
| 10    | V <sub>CLLow</sub>    | Low-level input voltage for clock            | -500.000 mV | 540.000 mV | -56.786 mV | -50.438 mV | -42.405 mV | 49.004 mV          | 4920  | -88.8%     | -107.8%    | Pass   |
| 11    | V <sub>DataLow</sub>  | Low-level input voltage for Data             | -500.000 mV | 540.000 mV | -55.069 mV | -49.177 mV | -35.569 mV | 51.321 mV          | 2467  | -89.0%     | -106.6%    | Pass   |
| 12    | V <sub>CLHigh</sub>   | High-level input voltage for clock           | 1.260 V     | 2.300 V    | 1.825 V    | 1.835 V    | 1.850 V    | 93.739 mV          | 4930  | 44.8%      | -19.6%     | Pass   |
| 13    | V <sub>DataHigh</sub> | High-level input voltage for Data            | 1.260 V     | 2.300 V    | 1.499 V    | 1.515 V    | 1.531 V    | 77.266 mV          | 2467  | 19.0%      | -33.4%     | Pass   |

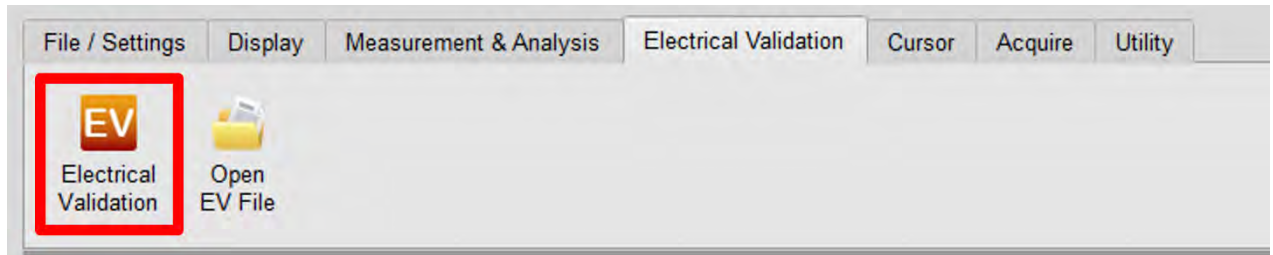
#### f<sub>CLK</sub> - Test Result: Pass

Description: Clock frequency

| Limit Min | Limit Max | Min       | Mean      | Max       | Standard Deviation | Count | Margin Min | Margin Max |
|-----------|-----------|-----------|-----------|-----------|--------------------|-------|------------|------------|
| 0.000 Hz  | 3.072 MHz | 3.027 MHz | 3.030 MHz | 3.034 MHz | 17.798 KHz         | 4430  | ---        | -1.2%      |

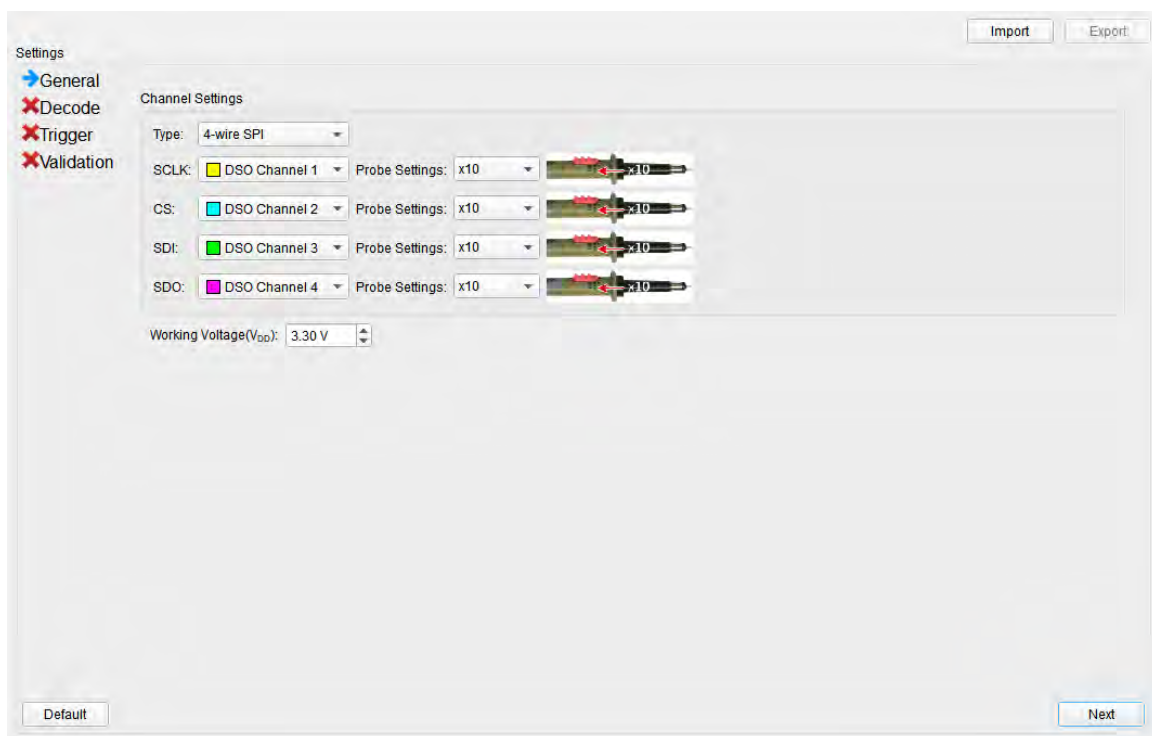


# SPI Electrical Validation Solution



## Settings Guide

### 1. General Settings

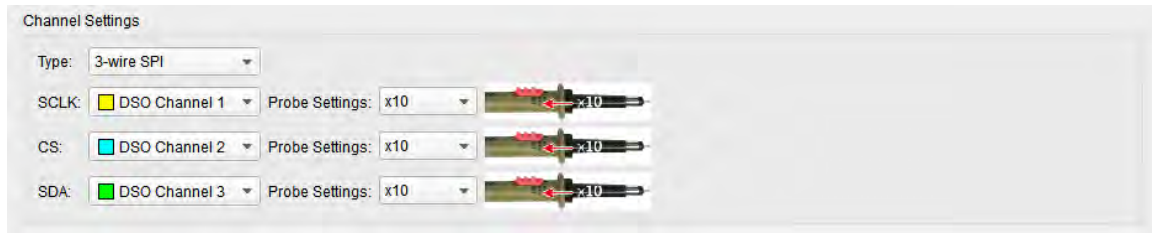


In the General Settings section, it is mandatory to select the type of SPI type, depending on your bus configuration (4-wire SPI or 3-wire SPI).

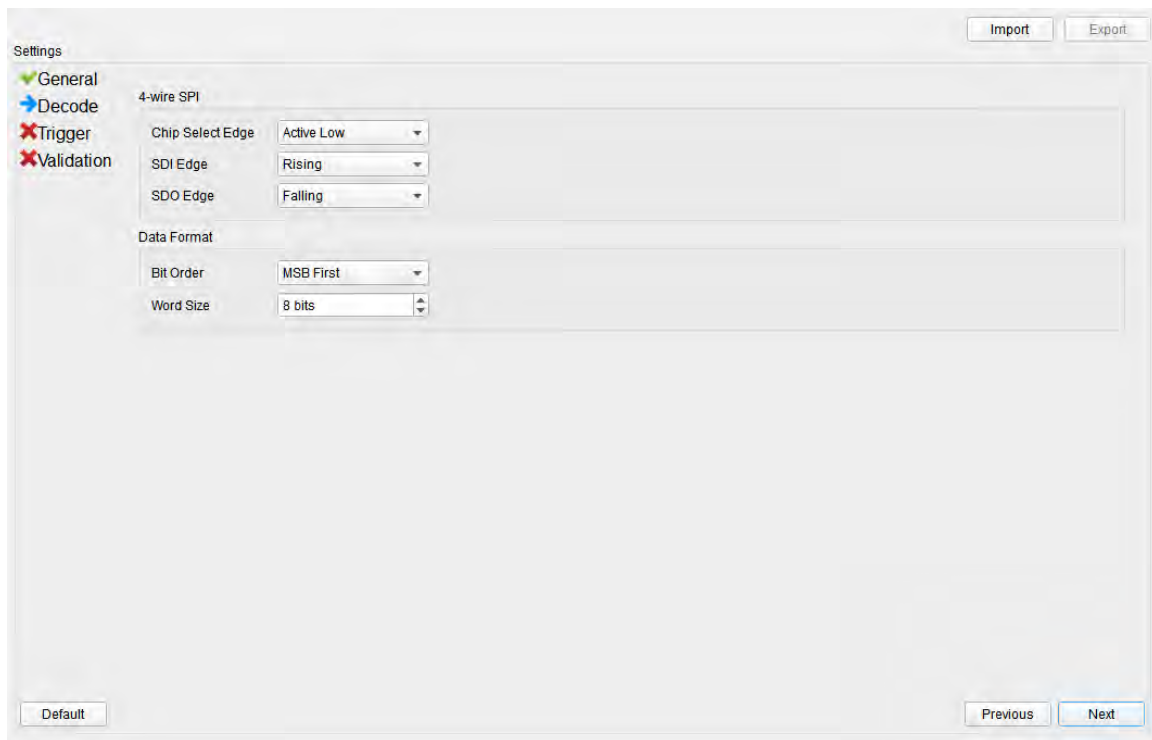
#### 4-wire Channel Setup



#### 3-wire Channel Setup

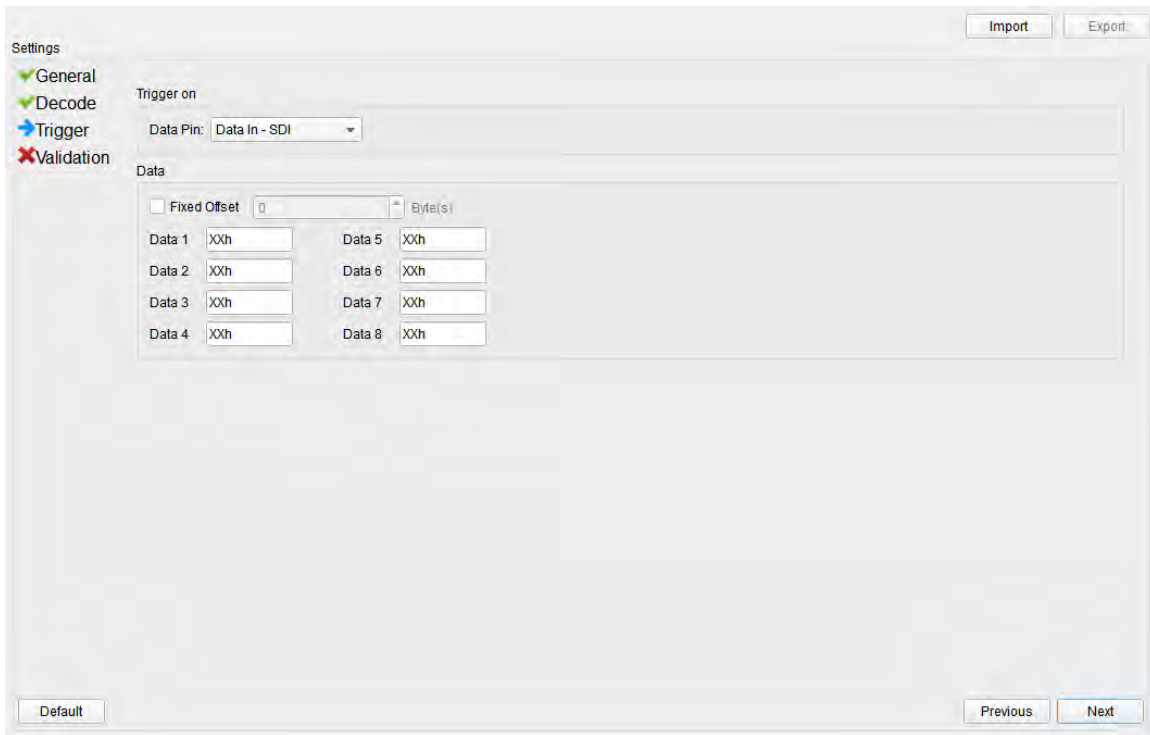


## 2. Decode Settings



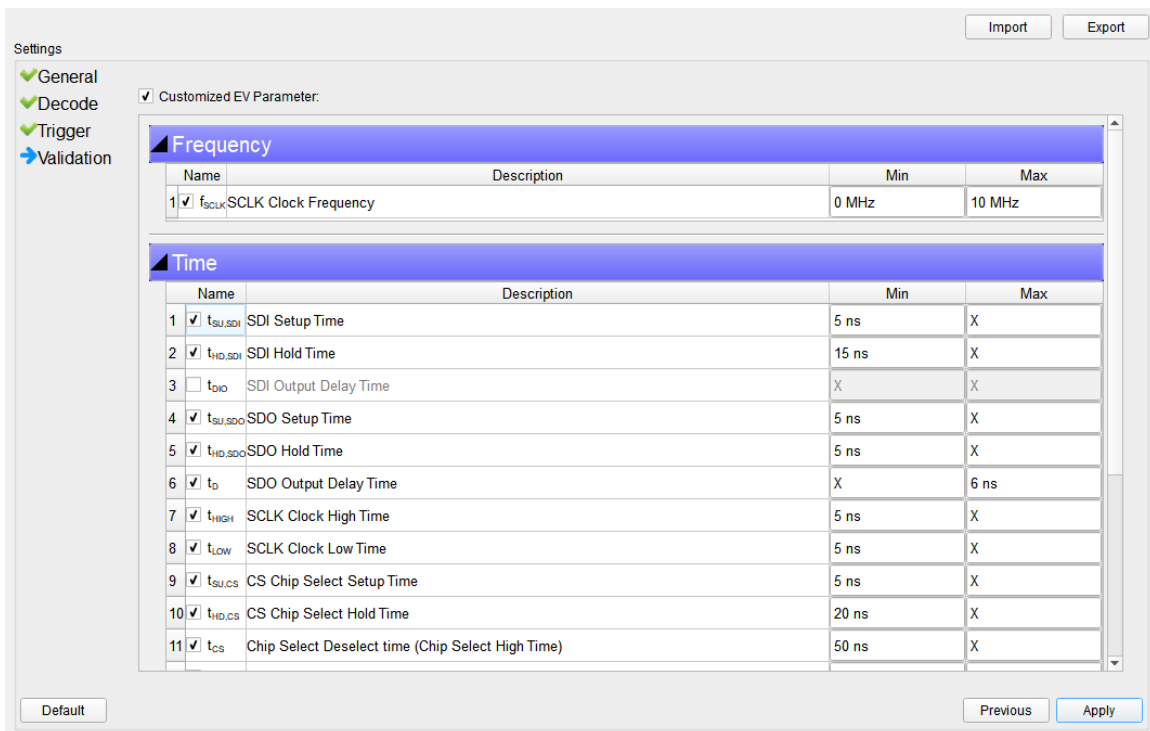
In the Decode Settings, it requires you to setup the SPI data format and the Latching Edge of each channel. The SPI data format set here is applied both to the Decode and Trigger Settings.

## 3. Trigger Settings



The data format is set on the previous page. The remaining setup is all about the data address and which data pin to trigger.

#### 4. Validation Settings



There are no standard measurement limits defined for SPI bus. Therefore, it is recommended to define your own limits while validate SPI signals.

This section displays 3 characteristics table, including

- Frequency
- Timing parameters
- Voltage requirements

All supported validation parameters' symbols and descriptions are listed in the table below.

### SPI Frequency Requirements

| Symbol            | Electrical Parameter |
|-------------------|----------------------|
| $f_{\text{SCLK}}$ | SCLK Clock Frequency |

### SPI Timing Requirements

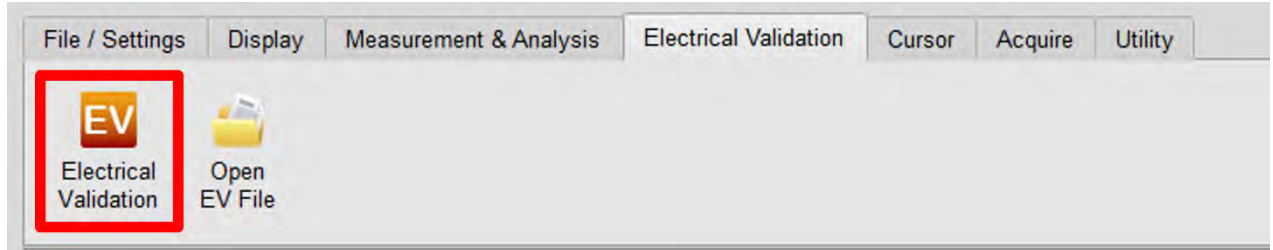
| Symbol              | Electrical Parameter                              |
|---------------------|---|
| $t_{\text{SU,SDI}}$ | SDI Setup Time                                    |
| $t_{\text{HD,SDI}}$ | SDI Hold Time                                     |
| $t_{\text{DIO}}$    | SDI Output Delay Time                             |
| $t_{\text{SU,SDO}}$ | SDO Setup Time                                    |
| $t_{\text{HU,SDO}}$ | SDO Hold Time                                     |
| $t_{\text{D}}$      | SDO Output Delay Time                             |
| $t_{\text{HIGH}}$   | SCLK High Time                                    |
| $t_{\text{LOW}}$    | SCLK Low Time                                     |
| $t_{\text{SU,CS}}$  | CS Chip Select Setup Time                         |
| $t_{\text{SU,CS}}$  | CS Chip Select Hold Time                          |
| $t_{\text{CS}}$     | Chip Select Deselect time (Chip Select High Time) |
| $t_{\text{CLKr}}$   | SCLK Clock Rise Time                              |
| $t_{\text{CLKf}}$   | SCLK Clock Fall Time                              |

### SPI Voltage Requirements

| Symbol          | Electrical Parameter      |
|-----------------|---------------------------|
| $V_{\text{IL}}$ | Low-Level Input Voltage   |
| $V_{\text{IH}}$ | High-level Input Voltage  |
| $V_{\text{OL}}$ | Low-level Output Voltage  |
| $V_{\text{OH}}$ | High-level Output Voltage |

# UART Electrical Validation Solution

## ■ Introduction:



Use an oscilloscope to do UART Electrical Validation to ensure that the UART meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

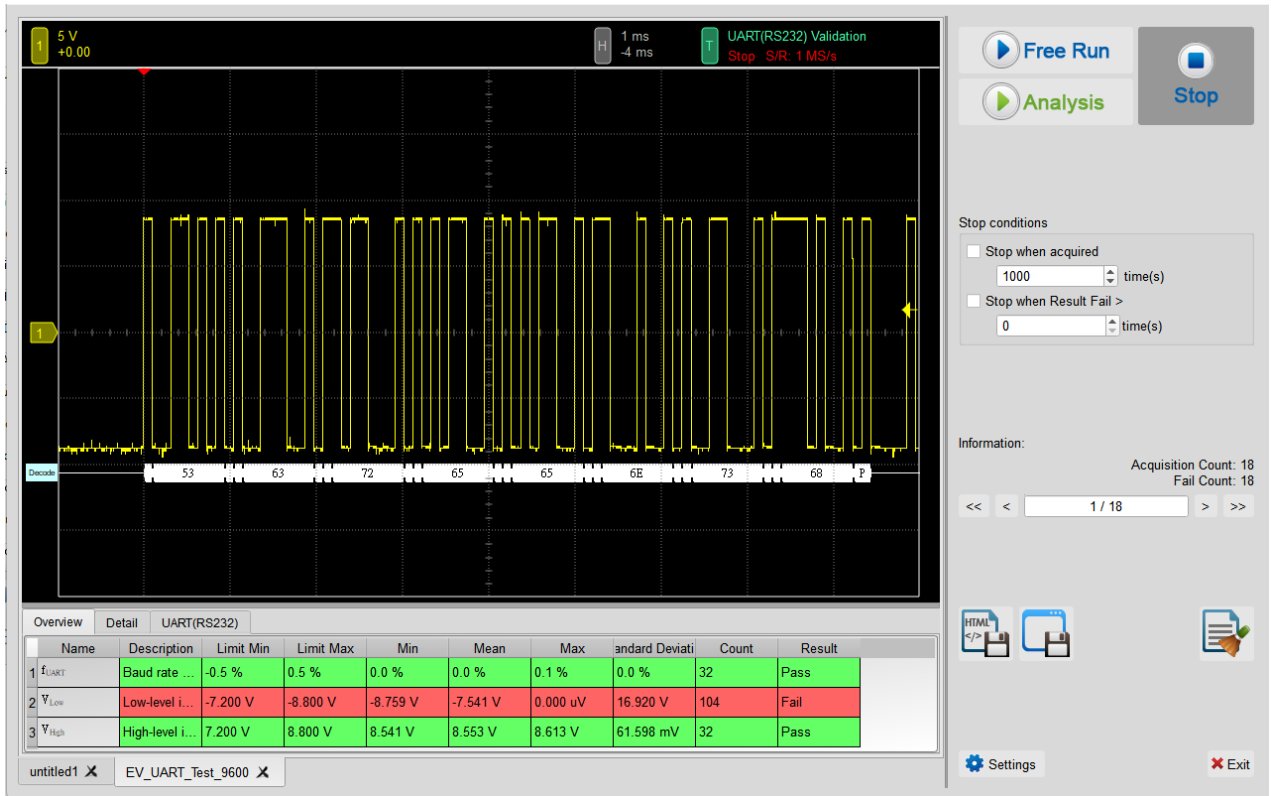
UART Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the UART Speed.

The report of common UART validation:

| Overview    |            |                 |           |           |          |          |          |                    |       |        |
|-------------|------------|-----------------|-----------|-----------|----------|----------|----------|--------------------|-------|--------|
| Detail      |            |                 |           |           |          |          |          |                    |       |        |
| UART(RS232) |            |                 |           |           |          |          |          |                    |       |        |
|             | Name       | Description     | Limit Min | Limit Max | Min      | Mean     | Max      | Standard Deviation | Count | Result |
| 1           | $f_{UART}$ | Baud rate ...   | -0.5 %    | 0.5 %     | 0.0 %    | 0.0 %    | 0.1 %    | 0.0 %              | 32    | Pass   |
| 2           | $V_{Low}$  | Low-level i...  | -7.200 V  | -8.800 V  | -8.759 V | -7.541 V | 0.000 uV | 16.920 V           | 104   | Fail   |
| 3           | $V_{High}$ | High-level i... | 7.200 V   | 8.800 V   | 8.541 V  | 8.553 V  | 8.613 V  | 61.598 mV          | 32    | Pass   |

Dedicated page for Electrical Validation:



1. Frequency: Clock speed
2. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
3. Voltage: V<sub>L</sub>, V<sub>H</sub>, etc.


## ■ UART Electrical Validation Settings:

### 1. General Settings: Channel sources, working voltage and speed

Settings

- General
- Decode
- Validation

Channel Settings

Data:  Probe Settings:  

Voltage High ( $V_{High}$ ):  Voltage Low ( $V_{Low}$ ):

Baud Rate

## 2. Decode Settings: UART decoding settings

Settings

- General
- Decode**
- Validation

Format

|           |           |
|-----------|-----------|
| Data Bits | Polarity  |
| 8         | Idle High |
| Parity    | Stop Bits |
| None      | 1         |

MSB First    Invert Bits

Report Size: 16

Default   Previous   Next

### 3. Electrical validation settings: Voltage, timing, frequency limitation

Settings

- General
- Decode
- Validation

Customized EV Parameter:

**Baud Rate**

| Name   | Description        | Min    | Max   |
|--|--------------------|--------|-------|
| <input checked="" type="checkbox"/> 1 $f_{UART}$ | Baud rate for UART | -0.5 % | 0.5 % |

**Time**

| Name   | Description    | Min            | Max             |
|--|----------------|----------------|-----------------|
| <input type="checkbox"/> 1 $t_r$                 | Edge rise time | X              | X               |
| <input type="checkbox"/> 2 $t_f$                 | Edge fall time | X              | X               |
| <input checked="" type="checkbox"/> 3 $t_{High}$ | High time      | 98.958 $\mu$ s | 109.375 $\mu$ s |
| <input checked="" type="checkbox"/> 4 $t_{Low}$  | Low time       | 98.958 $\mu$ s | 109.375 $\mu$ s |

**Voltage**

| Name   | Description              | Min    | Max    |
|--|--------------------------|--------|--------|
| <input checked="" type="checkbox"/> 1 $V_{Low}$  | Low-level input voltage  | -4.5 V | -5.5 V |
| <input checked="" type="checkbox"/> 2 $V_{High}$ | High-level input voltage | 4.5 V  | 5.5 V  |

Buttons: Default, Advance, Previous, Apply

### 4. Software electrical validation interface:

5 V  
+0.00

1 ms  
-4 ms

UART(RS232) Validation  
Stop S/R: 1 MS/s

Free Run  
Analysis  
Stop

Stop conditions

- Stop when acquired  
1000 time(s)
- Stop when Result Fail >  
0 time(s)

Information: Acquisition Count: 18  
Fail Count: 18

<< < 1 / 18 > >>

HTML  
Screenshot

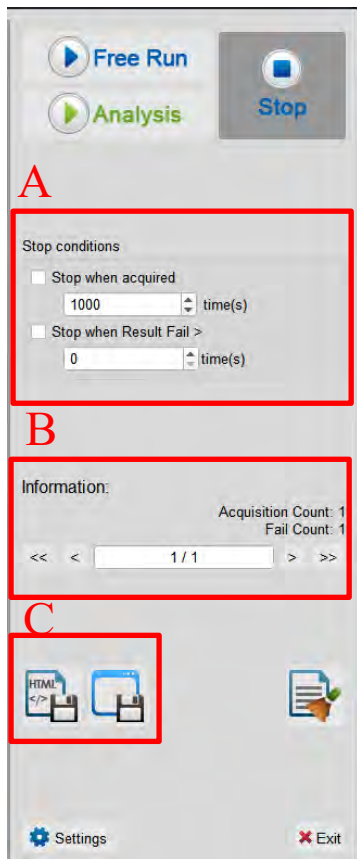
Settings Exit

Overview Detail UART(RS232)

| Timestamp  | State | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | ASCII    | Stop bit Error |
|------------|-------|----|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|----------|----------------|
| 1 1.104 ms | Tx    | 53 | 63 | 72 | 65 | 6E | 73 | 68 |    |    |    |     |     |     |     |     |     | Screensh |                |

untitled1 X EV\_UART\_Test\_9600 X

### 5. Software electrical validation control panel:



#### G. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

#### H. Information:

Select waveform

#### I. Save File:

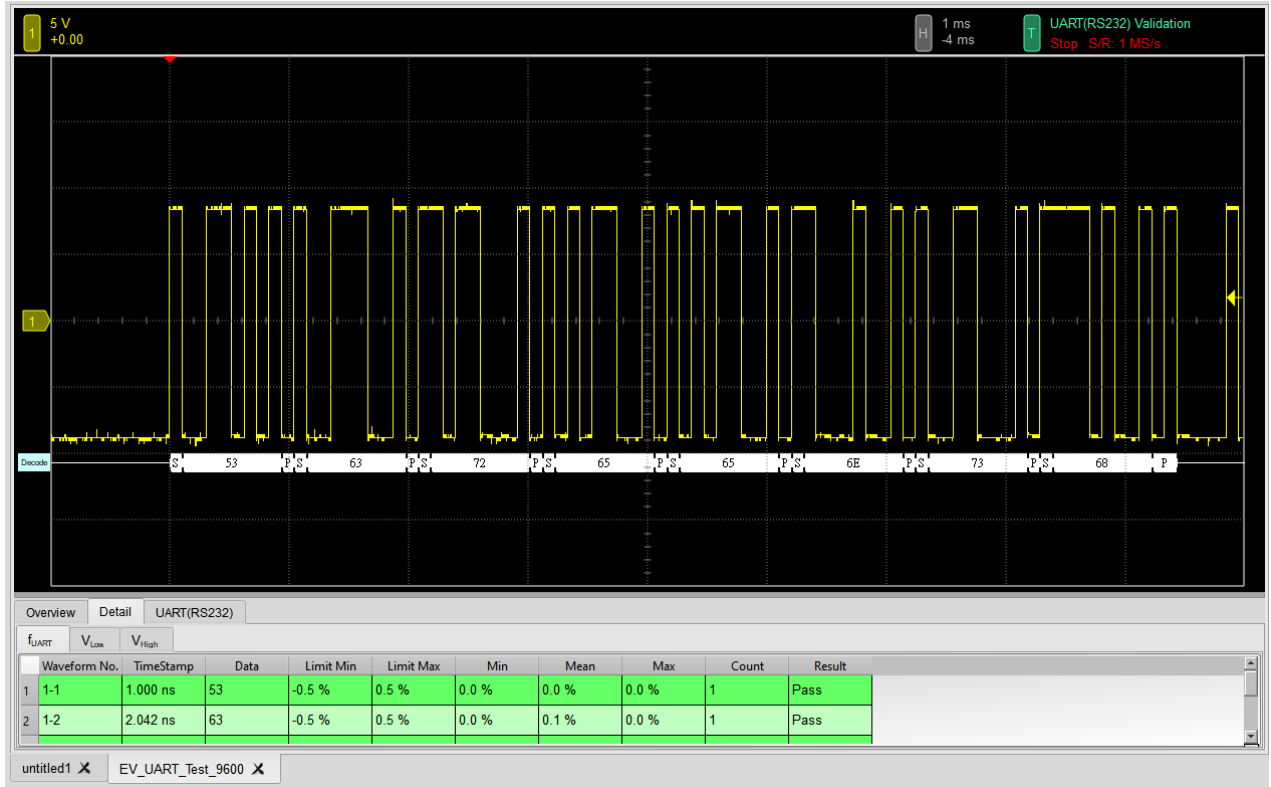
Save as Html

Save as .MOW(Software format)

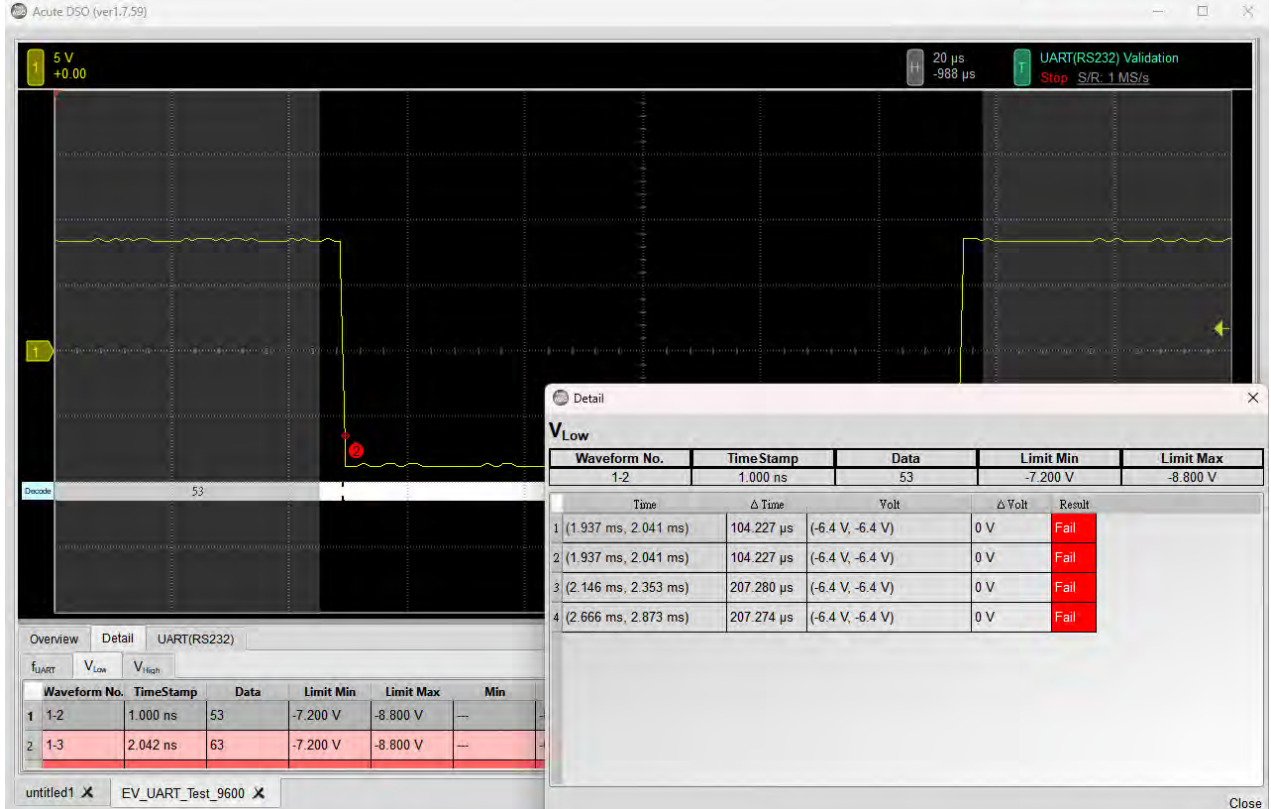
### 6. Overview Report:



## 7. Detail Report:



## 8. Reference Point Dialog & Waveform:



## 9. Html Report:



### Electrical Validation Report

|                                |                     |
|--------------------------------|---------------------|
| Test Instrument Model          | MSO3124V            |
| Test Instruments Serial Number | MSV31240017         |
| Test Date                      | 04-27-2023 15:07:32 |
| S/W Version                    | 1.0.25              |
| Protocol                       | UART(RS232)         |

#### Overview Results:

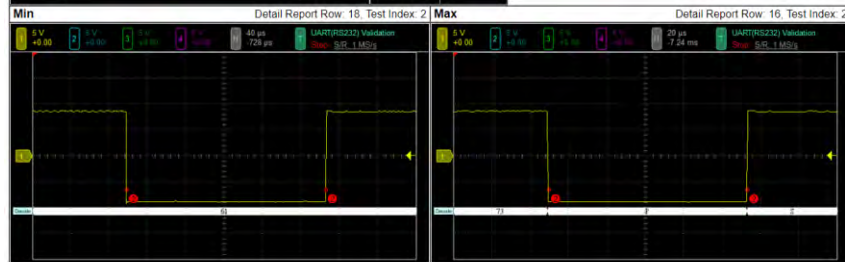
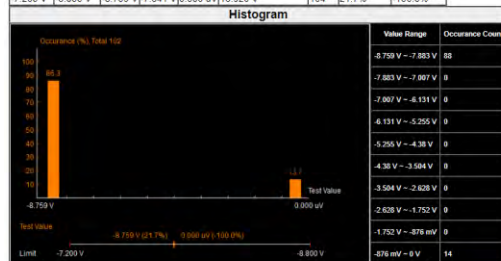
Total: 3  
Pass: 2  
Fail: 1

| Index Name | Description                                | Limit Min | Limit Max | Min      | Mean     | Max      | Standard Deviation | Count | Margin Min | Margin Max | Result |
|------------|--|-----------|-----------|----------|----------|----------|--------------------|-------|------------|------------|--------|
| 1          | UART Baud rate for UART                    | -0.5 %    | 0.5 %     | 0.0 %    | 0.0 %    | 0.1 %    | 0.0 %              | 32    | -100.0%    | -80.0%     | Pass   |
| 2          | V <sub>Low</sub> Low-level input voltage   | -7.200 V  | -8.800 V  | -8.759 V | -7.541 V | 0.000 uV | 16.920 V           | 104   | 21.7%      | -100.0%    | Fail   |
| 3          | V <sub>High</sub> High-level input voltage | 7.200 V   | 8.800 V   | 8.541 V  | 8.553 V  | 8.613 V  | 61.598 mV          | 32    | 18.6%      | -2.1%      | Pass   |

#### V<sub>Low</sub> - Test Result: Fail

Description: Low-level input voltage

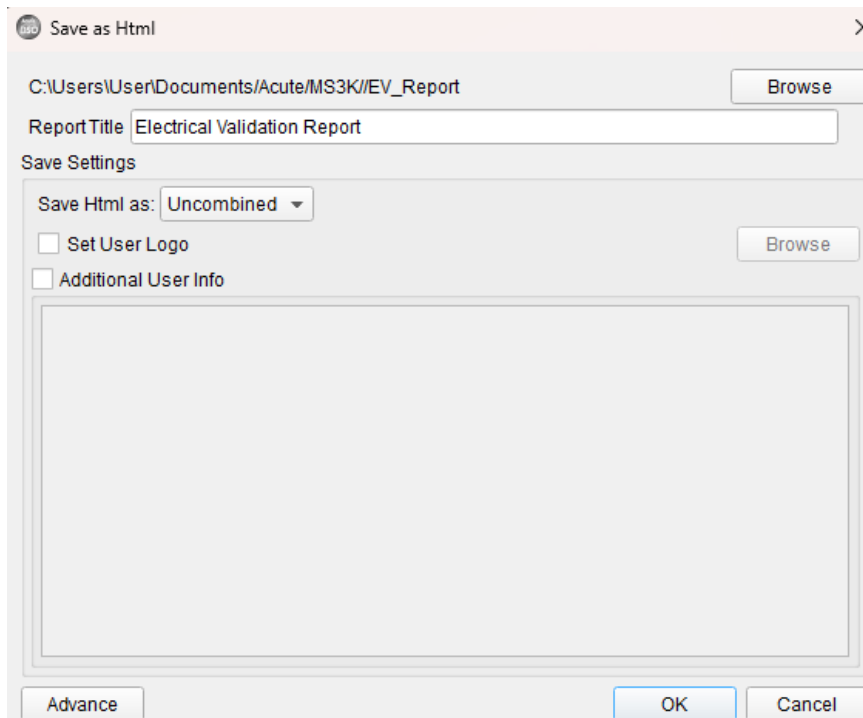
| Limit Min | Limit Max | Min      | Mean     | Max      | Standard Deviation | Count | Margin Min | Margin Max |
|-----------|-----------|----------|----------|----------|--------------------|-------|------------|------------|
| -7.200 V  | -8.800 V  | -8.759 V | -7.541 V | 0.000 uV | 16.920 V           | 104   | 21.7%      | -100.0%    |



# HTML Report Export

## ■ Introduction

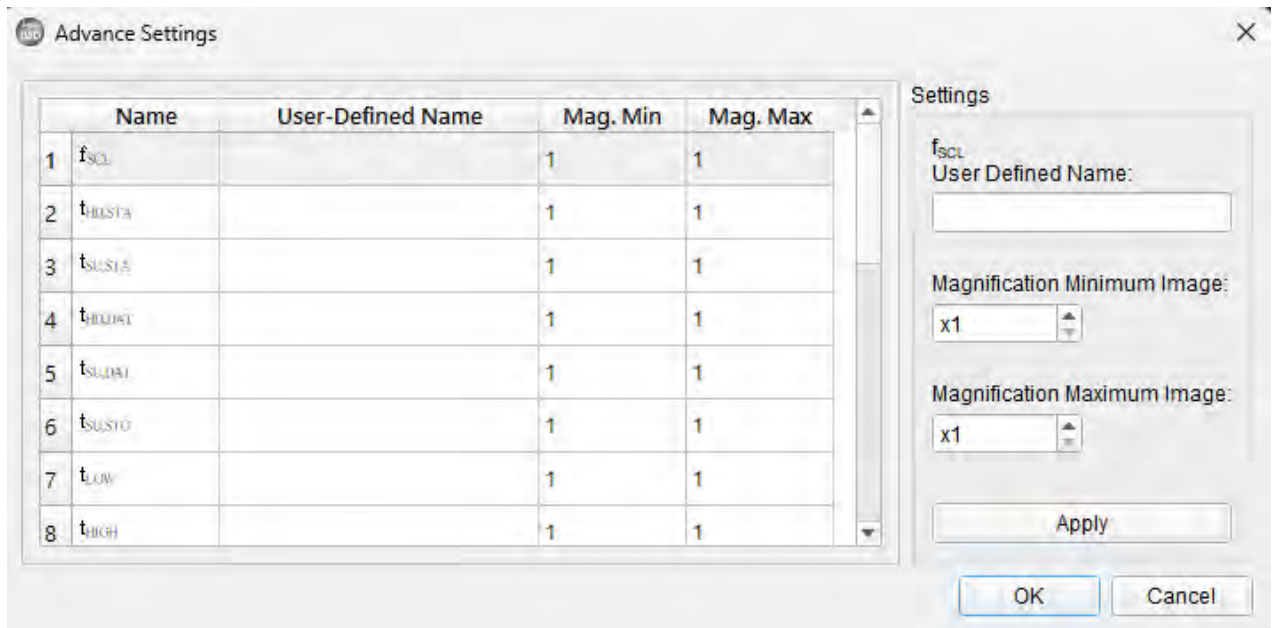
Every EV Testing includes Html Report exporting. The Html report contains every testing item, limitation, result, max/min value, histogram and waveform screenshots.



Save Settings:

- A. Save Html as: Uncombined/Combined file  
Uncombined: The images of the Html report will not be saved in Html file.  
Combined: The images are embedded in the Html report.
- B. Set User Logo:  
User can add their Logo to the report
- C. Additional User Info:  
This allows the user to type in any information that user want to put into the report.

Advance:



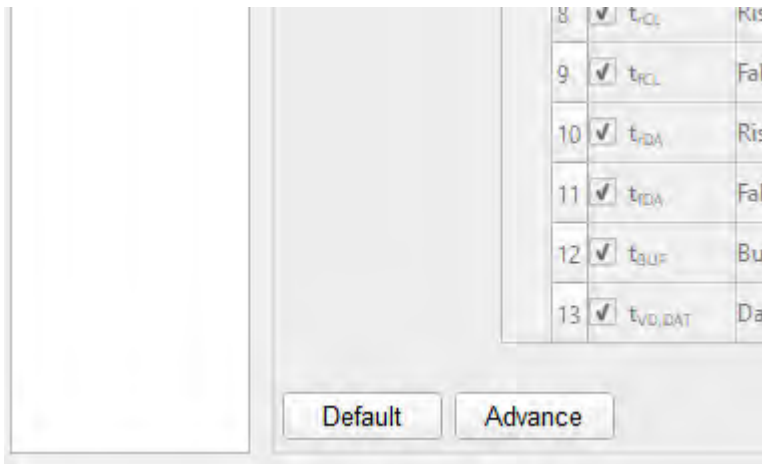
- A. User can adjust the name of the test item that will be displayed in Html report.
- B. User can also adjust the image magnification in Html report.

# Advanced Settings

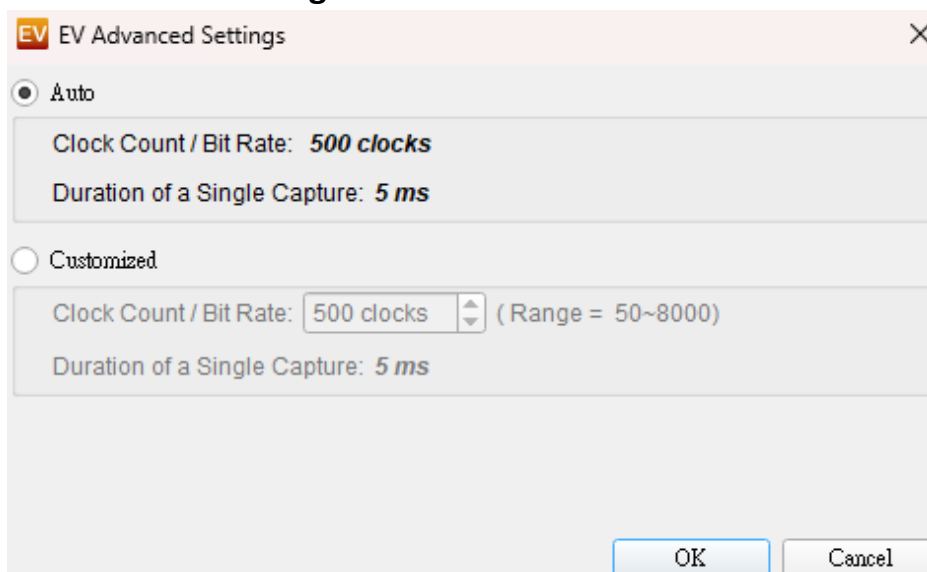
## ■ Introduction

EV Testing is able to increase or decrease the default capture timing for each acquisition. Different protocol default clock count or bit rate is not the same. Because the speed of the protocols & the packet length are not the same. But sometimes it needs more packet length. That is why Acute add an advanced settings to adjust the timing.

**\*Advance Button will only show in EV Parameter Settings State**



### EV Advanced Settings:



# MSO/TS3000 series 64-Channel cascading

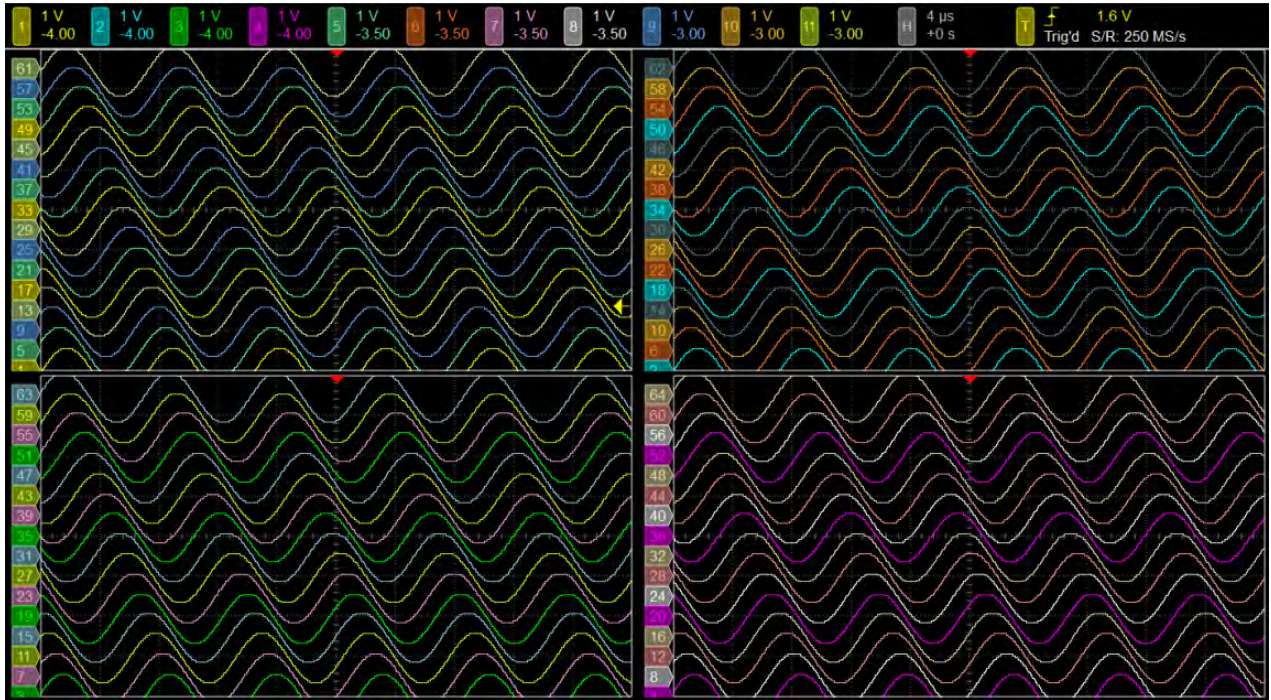
## ■ Introduction

One of the key features of the Acute MSO3K/TS3K oscilloscope is its multi-unit stacking capability, allowing for the stacking of up to 16 devices, achieving a maximum measurement capability of 64 channels at 250MS/s or 16 channels at 1GS/s simultaneously. In terms of its chassis design, the MSO3K/TS3K is specifically designed for stacking applications, featuring carefully designed positioning grooves that allow the oscilloscope to be perfectly aligned when stacked. Additionally, the oscilloscope's thermal performance has been thoroughly considered and includes dual-side heat vents to ensure there are no overheating issues during extended operation.

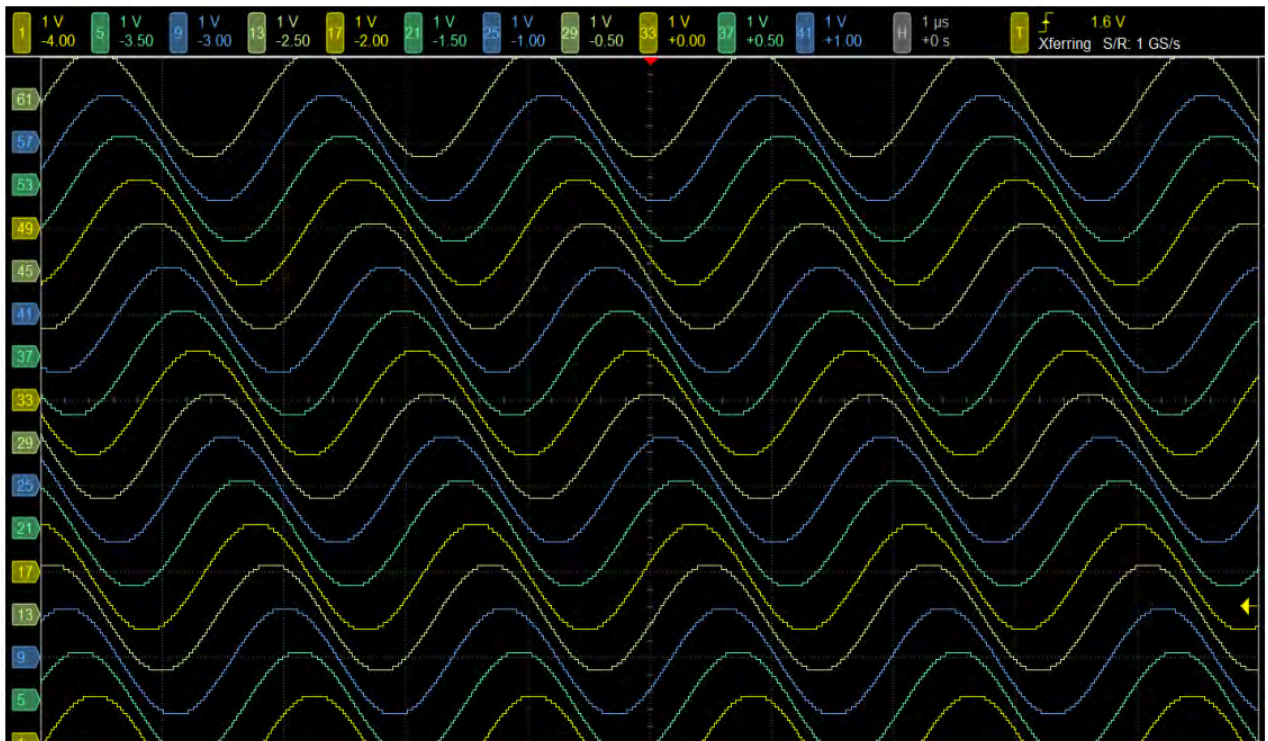
Regarding signal connections, users have the option to directly connect the test signal to the oscilloscope through standard BNC connectors or use passive probes or differential probes for more extensive measurements. Furthermore, Acute also offers a BNC to Probe Tip Adaptor, which can improve common measurement quality issues associated with traditional probes, ensuring users obtain the most accurate measurement results.

## ■ Software User Interface

### 1. 64Channel @ 250MS/s



### 2. 16Channel @ 1GS/s



## ■ Connection

### 1. Connect with BNC to BNC Probe



### 2. Connect with Passive Probe



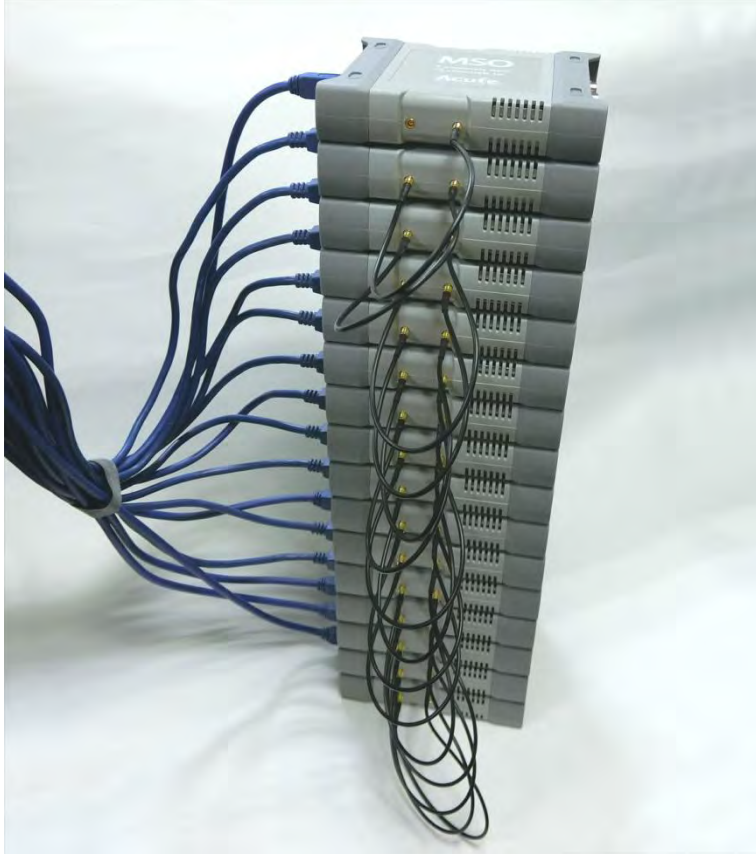
### 3. Connect with Passive Probe & BNC to Probe Tip Adaptor



### 4. Connect with High Voltage Differential Probe

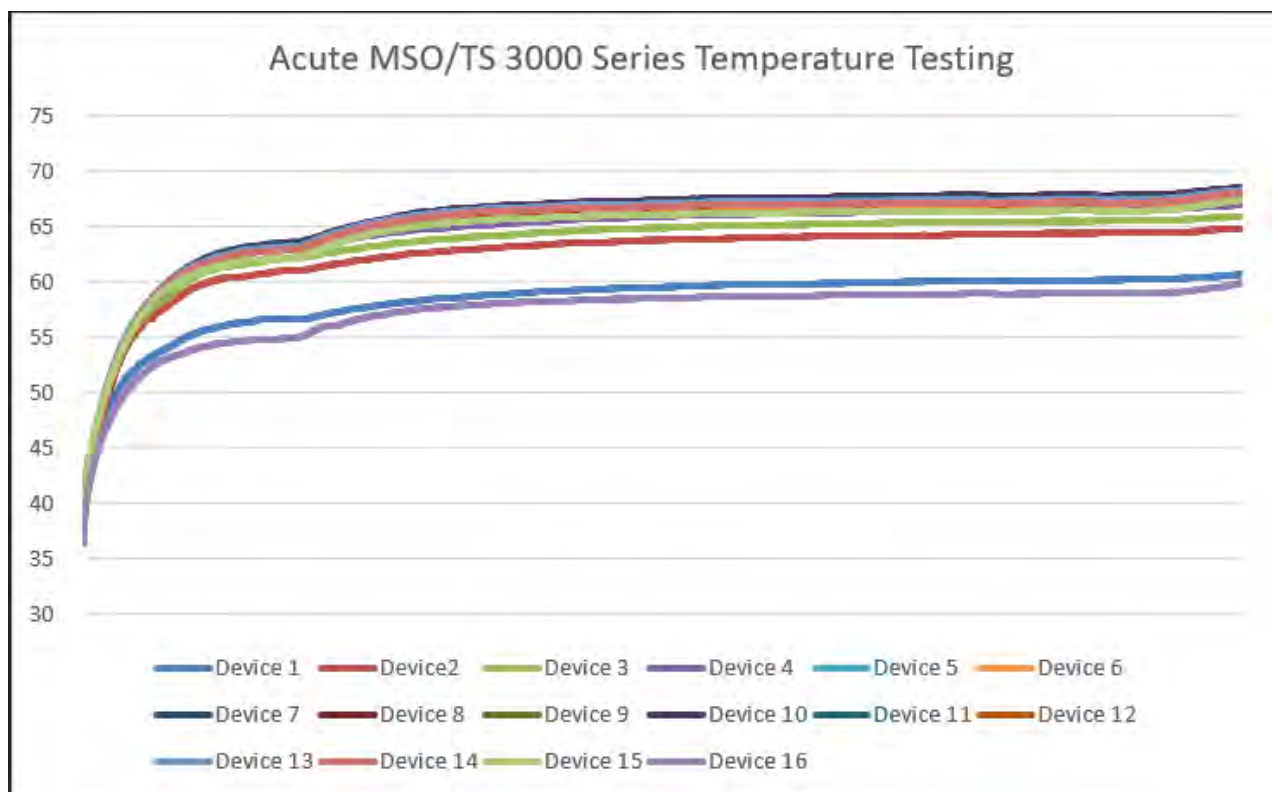


## 5. Cascading 16 Devices(64 Channels)



## ■ Cautions

1. The MSO3K/TS3K instrument operates on a USB 3.0 interface and consumes approximately 4.5 to 7.7 watts during operation. It is recommended to connect it to a USB 3.0 port at the rear of your computer or use a USB 3.0 hub with its own power supply to ensure optimal measurement quality.
2. The MSO3K/TS3K instrument has undergone internal testing and can operate for extended periods without overheating even in a stacked configuration. However, when using the instrument for an extended period in high-temperature or poorly ventilated environments, it is essential to monitor the operating temperature of the device and consider providing additional cooling measures if needed to prevent overheating (temperature exceeding 80 degrees Celsius) that could impact its operation.



3. When multiple units are stacked, there will be some level of phase difference between them due to differences in sampling rates. For example, at a 1GS/s sampling rate, the phase difference between the master unit and the first slave unit is  $< \pm 2\text{ns}$ , and between the master unit and the last slave unit is  $< \pm 3\text{ns}$ .

